MT6353 PMIC Datasheet

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.5V ~ 4.5V
- 5 buck converters and 28 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- 32K RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- Flexibility for various configurations of indicator LED current source: 2 ISINK
- SPI interface
- Li-ion battery charging function
- USB Battery Charging Specification ver 1.1/1.2 (BC1.x) Compliance
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 224-pin MFC VFBGA package

1.2 Applications

MT6353 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6353 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 5 buck converters and 28 LDOs optimized for specific 2G/3G/4G smart phone subsystems.

LED drivers support up to 2 channels of LEDs with independent control. Flexible control includes register mode, PWM mode and breath mode.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6353 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6353 adopts SPI interface and 2 SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6353 is available in a 224-pin VFBGA package. The operating temperature ranges from -30 to +85°C.

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1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6353V/A		-30 ~ +85°C	VFBGA 224L

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1.5 Top Marking Definition

MT6353V/A

YYWW: Date code

$: Random code

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1.6 Pin Assignments and Descriptions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VPA	GND_VPA		VBAT_VPROC	GND_VPROC	VPROC	VPROC	VCORE2		VBAT_VCORE		VCORE	VS1	VBAT_VS1		AVDD20_LDO5	AVDD20_LDO3
B	VBAT_VPA	GND_VPROC_FB	VBAT_VPROC	VBAT_VPROC	GND_VPROC	GND_VPROC	VPROC	VCORE2	VBAT_VCORE2	VBAT_VCORE	GND_VCORE	VCORE	VS1	VBAT_VS1	VRF18	VRF18	VIO18
C		VPROC_FB	VCORE2_FB	VBAT_VPROC	GND_VPROC	GND_VPROC	VPROC	VCORE2	VBAT_VCORE2	GND_VCORE2	GND_VCORE	VCORE	GND_VS1	VRF12	VCN18	VIO18	AVDD20_LDO2
D	SPK_N		GND_VCORE2_FB	VPA_FB	GND_SMPS	GND_LDO	VPROC	GND_LDO	GND_VCORE2	GND_VCORE2	GND_VCORE	GND_LDO	GND_VS1	GND_LDO	VCAMIO		VDRAM
E	SPK_P	GND_ISINK	ISINK0	ISINK1	VBAT_SMPS	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	VCAMD	AVDD20_LDO4	VSRAM_PROC	
F	VBAT_SPK	AU_FLYN	GND_SPK		VBAT_LDO6	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	AVDD20_LDO1	VCORE_FB	GND_VCORE_FB	VMCH
G		AU_FLYP	AVSS18N_AUD			GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	VMC	VS1_FB	VBAT_LDO5	
H	HPR	HPL	AVSS18_AUD	AVDD18_AUD		GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	VSIM1	VSIM2	VBAT_LDO4
J	AVSS28_AUD	HSN	AU_REFN		CLK26M	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	GND_LDO	VIBR	
K		HSP		AU_VIN1_P	AVDD28_AUD						GND_LDO	GND_LDO	GND_LDO	GND_LDO	VLDO28	VIO28	VBAT_LDO3
L		AU_VIN2_P	AU_VIN0_P	AU_VIN1_N		VDRV	VAUD28	AUD_CLK	DCXO32K_EN	VRTC28	RTC32K_1V8_1	SPI_CLK	DVDD18_DIG			XO_WCN	VEMC33
M	AU_MICBIAS0	AU_VIN2_N	AU_VIN0_N		UVLO_VTH	VCAMA	AUD_DAT_MOSI	AUD_DAT_MISO	SPI_MISO		WDTRSTB_IN	DVDD18_IO	DVSS18_IO		EXT_PMIC_EN	XO_CEL	
N	AU_MICBIAS1	ACCDET		CHRLDO	CS_P	RESETB	TREF		XMODE	SPI_CSN			TYPEC_CC1			XO_NFC	XO_SOC
P		FCHR_ENB	PCHR_LED	VCDT	CS_N		VCN28		SPI_MOSI			AVSS18_AUXADC	TYPEC_CC2	VTCXO24	VXO22	AVSS22_XO	AVSS22_XOBUF
R	BATSNS	VSYSSNS	CHG_DP	CHG_DM	PMU_TESTMODE	VBAT_LDO1	VTCXO28	RTC32K_2V8	XIN	GND_RTC	SRCLKEN_IN1	AVDD18_AUXADC	AUXADC_VIN	VCN33			XTAL1
T	ISENSE	BATON	VREF	GND_VREF	PWRKEY			VAUX18	XOUT		RTC32K_1V8_0		SRCLKEN_IN0	VUSB33	VBAT_LDO2	FSOURCE	XTAL2

Figure 1-1. MT6353 MFC VFBGA 224 (7.0*6.6mm) pin assignment

Table 1-1. MT6353 pin descriptions

Ball	Symbol	I/O	Description
A4, B3, B4, C4	VBAT_VPROC	PWR	Power supply of VPROC
A6, A7, B7, C7, D7	VPROC	O	SW node of VPROC
A5, B5, B6, C5, C6	GND_VPROC	GND	VPROC ground
C2	VPROC_FB	I	BUCK VPROC feedback pin
B2	GND_VPROC_FB	I	Remote sense on ground of VPROC
A10, B10	VBAT_VCORE	PWR	Power supply of VCORE
A12, B12, C12	VCORE	O	SW node of VCORE
B11, C11, D11	GND_VCORE	GND	VCORE ground
F15	VCORE_FB	I	BUCK VCORE feedback pin
F16	GND_VCORE_FB	I	Remote sense on ground of VCORE
B9, C9	VBAT_VCORE2	PWR	Power supply of VCORE2
A8, B8, C8	VCORE2	O	SW node of VCORE2
C10, D10, D9	GND_VCORE2	GND	VCORE2 ground
C3	VCORE2_FB	I	BUCK VCORE2 feedback pin
D3	GND_VCORE2_FB	I	Remote sense on ground of VCORE2
A14, B14	VBAT_VS1	PWR	Power supply of VS1
A13, B13	VS1	O	SW node of VS1
C13, D13	GND_VS1	GND	VS1 ground
G15	VS1_FB	I	BUCK VS1 feedback pin

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Ball	Symbol	I/O	Description
B1	VBAT_VPA	PWR	Power supply of VPA
A1	VPA	O	SW node of VPA
A2	GND_VPA	GND	VPA ground
D4	VPA_FB	I	BUCK VPA feedback pin
E5	VBAT_SMPS	PWR	Power supply of buck controller
D5	GND_SMPS	GND	buck controller ground
P14	VTCXO24	O	VTCXO24 output voltage
R7	VTCXO28	O	VTCXO28 output voltage
P15	VXO22	O	VXO22 output voltage
B15, B16	VRF18	O	VRF18 output voltage
C14	VRF12	O	VRF12 output voltage
C15	VCN18	O	VCN18 output voltage
P7	VCN28	O	VCN28 output voltage
R14	VCN33	O	VCN33 output voltage
M6	VCAMA	O	VCAMA output voltage
E14	VCAMD	O	VCAMD output voltage
D15	VCAMIO	O	VCAMIO output voltage
K15	VLDO28	O	VCAMAF output voltage
L7	VAUD28	O	VAUD28 output voltage
T8	VAUX18	O	VAUX18 output voltage
E16	VSRAM_PROC	O	VSRAM_PROC output voltage
D17	VDRAM	O	VDRAM output voltage
L17	VEMC33	O	VEMC output voltage
G14	VMC	O	VMC output voltage
F17	VMCH	O	VMCH output voltage
T14	VUSB33	O	VUSB33 output voltage
H15	VSIM1	O	VSIM1 output voltage
H16	VSIM2	O	VSIM2 output voltage
J16	VIBR	O	VIBR output voltage
B17, C16	VIO18	O	VIO18 output voltage
K16	VIO28	O	VIO28 output voltage
L10	VRTC28	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
R10	GND_RTC	GND	RTC ground
N7	TREF	O	Battery interface
L13	DVDD18_DIG	O	VDIG18 output voltage
M12	DVDD18_IO	PWR	Digital IO power
M13	DVSS18_IO	GND	Digital IO power GND
R6	VBAT_LDO1	PWR	Power supply input of LDO group1
T15	VBAT_LDO2	PWR	Power supply input of LDO group2
K17	VBAT_LDO3	PWR	Power supply input of LDO group3
H17	VBAT_LDO4	PWR	Power supply input of LDO group4
G16	VBAT_LDO5	PWR	Power supply input of LDO group5
F5	VBAT_LDO6	PWR	Power supply input of LDO group6
F14	AVDD20_LDO1	PWR	2V power supply of SLDO1
C17	AVDD20_LDO2	PWR	2V power supply of SLDO2
A17	AVDD20_LDO3	PWR	2V power supply of SLDO3
E15	AVDD20_LDO4	PWR	2V power supply of SLDO4
A16	AVDD20_LDO5	PWR	2V power supply of SLDO5
L6	VDRV	O	Charger current drive output
P4	VCDT	I	Fractional charger input voltage for charger detection

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Ball	Symbol	I/O	Description
R4	CHG_DM	I	USB D- for BC1.1 standard
R3	CHG_DP	I	USB D+ for BC1.1 standard
N4	CHRLDO	O	CHRLDO output voltage
T1	ISENSE	I	Positive terminal for battery's charging current sensing resistor
R1	BATSNS	I	Negative terminal for battery's charging current sensing resistor
P2	FCHR_ENB	I	Force charging disable pin(Merge with HOMEKEY,Same as MT6323)
T2	BATON	I	Battery NTC pin for battery and its temperature sensing
M5	UVLO_VTH	I	UVLO threshold control pin
P5	CS_N	I	Fuel gauge ADC input pin
N5	CS_P	I	Fuel gauge ADC input pin
N13	TYPEC_CC1	I	TYPEC input 1
P13	TYPEC_CC2	I	TYPEC input 2
E3	ISINK0	I	ISINK channel 0
E4	ISINK1	I	ISINK channel 1
P3	PCHR_LED	I	Pre-Charge Indicator
E2	GND_ISINK	GND	ISINK ground
T11	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
L11	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
R8	RTC32K_2V8	O	VRTC domain 32kHz clock output
R9	XIN	IO	32K crystal connection port while using crystal to generate 32kHz clock
T9	XOUT	IO	32K crystal connection port while using crystal to generate 32kHz clock
L12	SPI_CLK	I	SPI control interface
N10	SPI_CSN	IO	SPI control interface
M9	SPI_MISO	IO	SPI control interface
P9	SPI_MOSI	IO	SPI control interface
M11	WDTRSTB_IN	I	Watchdog reset from AP
N6	RESETB	O	System reset release signal
T13	SRCLKEN_IN0	I	Source clock enable pin 0
R11	SRCLKEN_IN1	I	Source clock enable pin 1
M15	EXT_PMIC_EN	IO	Ext chip MT6311/MT6312 enable pin
T3	VREF	O	Bandgap reference voltage
T4	GND_VREF	GND	Ground for bandgap
R2	VSYSSNS	PWR	VSYS supply input for internal block and UVLO detection
T16	FSOURCE	PWR	EFUSE power source
R5	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
T5	PWRKEY	I	PWRKEY button
R13	AUXADC_VIN	I	AUXADC input
R12	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
P12	AVSS18_AUXADC	GND	AUXADC ground
N2	ACCDET	I	Accessory detection input 1
F2	AU_FLYN	O	Flying capacitor bottom
G2	AU_FLYP	O	Flying capacitor top
M1	AU_MICBIAS0	O	Microphone Bias 0
N1	AU_MICBIAS1	O	Microphone Bias 1
J3	AU_REFN	GND	Audio reference ground

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Ball	Symbol	I/O	Description
M3	AU_VIN0_N	I	Microphone channel 0 negative input
L3	AU_VIN0_P	I	Microphone channel 0 positive input
L4	AU_VIN1_N	I	Microphone channel 1 negative input
K4	AU_VIN1_P	I	Microphone channel 1 positive input
M2	AU_VIN2_N	I	Microphone channel 2 negative input
L2	AU_VIN2_P	I	Microphone channel 2 positive input
L8	AUD_CLK	I	Audio control interface
M8	AUD_DAT_MISO	IO	Audio control interface
M7	AUD_DAT_MOSI	IO	Audio control interface
H4	AVDD18_AUD	PWR	1.8V power supply of Audio
K5	AVDD28_AUD	PWR	Power supply of Audio UL
H3	AVSS18_AUD	GND	Audio DL ground
G3	AVSS18N_AUD	PWR	Audio -1.8V supply
J1	AVSS28_AUD	GND	Audio UL ground
F1	VBAT_SPK	PWR	Power supply of SPK
D1	SPK_N	O	Negative output of internal speaker amp
E1	SPK_P	O	Positive output of internal speaker amp
F3	GND_SPK	GND	GND of internal speaker amp
J5	CLK26M	I	26MHz clock input
H2	HPL	O	Earphone left channel output
H1	HPR	O	Earphone right channel output
J2	HSN	O	Handset negative output
K2	HSP	O	Handset positive output
P16	AVSS22_XO	GND	Ground for XO
P17	AVSS22_XOBUF	GND	Ground for XO
R17	XTAL1	I	XTAL input 1
T17	XTAL2	I	XTAL input 2
N17	XO_SOC	O	26MHz output to SOC
L16	XO_WCN	O	26MHz output to Conn. RF
M16	XO_CEL	O	26MHz output to Cell. RF
N16	XO_NFC	O	26MHz output to NFC
L9	DCXO32K_EN	I	Config HW pin
N9	XMODE	I	Config HW pin
D12, D14, D6, D8, E10, E11, E12, E13, E6, E7, E8, E9, F10, F11, F12, F13, F6, F7, F8, F9, G10, G11, G12, G1, G6, G7, G8, G9, H10, H11, H12, H13, H14, H6, H7, H8, H9, J10, J11, J12, J13, J14, J15, J6, J7, J8, J9, K11 ,K12, K13, K14	GND_LDO	GND	LDO ground

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery Pin input voltage range				4.5	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

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2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		42.8[1]		°C/W

Note: The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-9 condition.

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2.3 Pin Voltage Range

The table below lists operation rang voltages for all MT6353 I/O pins.

Table 2-2. Pin voltage range

Ball	Symbol	Voltage range	Unit
A4, B3, B4, C4	VBAT_VPROC	0 ~ 4.5	v
A6, A7, B7, C7, D7	VPROC	0 ~ 4.5	v
A5, B5, B6, C5, C6	GND_VPROC	0	v
C2	VPROC_FB	0 ~ 4.5	v
B2	GND_VPROC_FB	0	v
A10, B10	VBAT_VCORE	0 ~ 4.5	v
A12, B12, C12	VCORE	0 ~ 4.5	v
B11, C11, D11	GND_VCORE	0	v
F15	VCORE_FB	0 ~ 4.5	v
F16	GND_VCORE_FB	0	v
B9, C9	VBAT_VCORE2	0 ~ 4.5	v
A8, B8, C8	VCORE2	0 ~ 4.5	v
C10, D10, D9	GND_VCORE2	0	v
C3	VCORE2_FB	0 ~ 4.5	v
D3	GND_VCORE2_FB	0	v
A14, B14	VBAT_VS1	0 ~ 4.5	v
A13, B13	VS1	0 ~ 4.5	v
C13, D13	GND_VS1	0	v
G15	VS1_FB	0 ~ 4.5	v
B1	VBAT_VPA	0 ~ 4.5	v
A1	VPA	0 ~ 4.5	v
A2	GND_VPA	0	v
D4	VPA_FB	0 ~ 4.5	v
E5	VBAT_SMPS	0 ~ 4.5	v
D5	GND_SMPS	0	v
P14	VTCXO24	0 ~ 4.5	v
R7	VTCXO28	0 ~ 4.5	v
P15	VXO22	0 ~ 4.5	v
B15, B16	VRF18	0 ~ 4.5	v
C14	VRF12	0 ~ 4.5	v
C15	VCN18	0 ~ 4.5	v
P7	VCN28	0 ~ 4.5	v
R14	VCN33	0 ~ 4.5	v
M6	VCAMA	0 ~ 4.5	v
E14	VCAMD	0 ~ 1.98	v
D15	VCAMIO	0 ~ 4.5	v
K15	VLDO28	0 ~ 4.5	v
L7	VAUD28	0 ~ 4.5	v
T8	VAUX18	0 ~ 4.5	v
E16	VSRAM_PROC	0 ~ 1.98	v

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Ball	Symbol	Voltage range	Unit
D17	VDRAM	0 ~ 4.5	v
L17	VEMC33	0 ~ 4.5	v
G14	VMC	0 ~ 4.5	v
F17	VMCH	0 ~ 4.5	v
T14	VUSB33	0 ~ 4.5	v
H15	VSIM1	0 ~ 4.5	v
H16	VSIM2	0 ~ 4.5	v
J16	VIBR	0 ~ 3.3	v
B17, C16	VIO18	0 ~ 4.5	v
K16	VIO28	0 ~ 4.5	v
L10	VRTC28	0 ~ 4.5	v
R10	GND_RTC	0	v
N7	TREF	0 ~ 1.98	v
L13	DVDD18_DIG	0 ~ 1.98	v
M12	DVDD18_IO	0 ~ 1.98	v
M13	DVSS18_IO	0	v
R6	VBAT_LDO1	0 ~ 4.5	v
T15	VBAT_LDO2	0 ~ 4.5	v
K17	VBAT_LDO3	0 ~ 4.5	v
H17	VBAT_LDO4	0 ~ 4.5	v
G16	VBAT_LDO5	0 ~ 4.5	v
F5	VBAT_LDO6	0 ~ 4.5	v
F14	AVDD20_LDO1	0 ~ 2.42	v
C17	AVDD20_LDO2	0 ~ 2.42	v
A17	AVDD20_LDO3	0 ~ 2.42	v
E15	AVDD20_LDO4	0 ~ 2.42	v
A16	AVDD20_LDO5	0 ~ 2.42	v
L6	VDRV	0 ~ 4.5	v
P4	VCDT	0 ~ 1.8	v
R4	CHG_DM	0 ~ 4.5	v
R3	CHG_DP	0 ~ 4.5	v
N4	CHRLDO	0 ~ 3.08	v
T1	ISENSE	0 ~ 4.5	v
R1	BATSNS	0 ~ 4.5	v
P2	FCHR_ENB	0 ~ 4.5	v
T2	BATON	0 ~ 4.5	v
M5	UVLO_VTH	0 ~ 3.3	v
P5	CS_N	0 ~ 0.1	v
N5	CS_P	0 ~ 0.1	v
N13	TYPEC_CC1	0 ~ 5.5	v
P13	TYPEC_CC2	0 ~ 5.5	v
E3	ISINK0	0 ~ 4.5	v
E4	ISINK1	0 ~ 4.5	v
P3	PCHR_LED	0 ~ 4.5	v
E2	GND_ISINK	0	v
T11	RTC32K_1V8_0	0 ~ 1.98	v

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Ball	Symbol	Voltage range	Unit
L11	RTC32K_1V8_1	0 ~ 1.98	v
R8	RTC32K_2V8	0 ~ 3.08	v
R9	XIN	0 ~ 3.08	v
T9	XOUT	0 ~ 3.08	v
L12	SPI_CLK	0 ~ 1.98	v
N10	SPI_CSN	0 ~ 1.98	v
M9	SPI_MISO	0 ~ 1.98	v
P9	SPI_MOSI	0 ~ 1.98	v
M11	WDTRSTB_IN	0 ~ 1.98	v
N6	RESETB	0 ~ 1.98	v
T13	SRCLKEN_IN0	0 ~ 1.98	v
R11	SRCLKEN_IN1	0 ~ 1.98	v
M15	EXT_PMIC_EN	0 ~ 4.5	v
T3	VREF	0 ~ 1.32	v
T4	GND_VREF	0	v
R2	VSYSSNS	0 ~ 4.5	v
T16	FSOURCE	0 ~ 1.98	v
R5	PMU_TESTMODE	0 ~ 4.5	v
T5	PWRKEY	0 ~ 4.5	v
R13	AUXADC_VIN	0 ~ 1.98	v
R12	AVDD18_AUXADC	0 ~ 1.98	v
P12	AVSS18_AUXADC	0	v
N2	ACCDET	0 ~ 3.08	v
F2	AU_FLYN	-1.98 ~ 0	v
G2	AU_FLYP	0 ~ 1.8	v
M1	AU_MICBIAS0	0~3.08	v
N1	AU_MICBIAS1	0~3.08	v
J3	AU_REFN	0	v
M3	AU_VIN0_N	0~3.08	v
L3	AU_VIN0_P	0~3.08	v
L4	AU_VIN1_N	0~3.08	v
K4	AU_VIN1_P	0~3.08	v
M2	AU_VIN2_N	0~3.08	v
L2	AU_VIN2_P	0~3.08	v
L8	AUD_CLK	0 ~ 1.98	v
M8	AUD_DAT_MISO	0 ~ 1.98	v
M7	AUD_DAT_MOSI	0 ~ 1.98	v
H4	AVDD18_AUD	0 ~ 1.98	v
K5	AVDD28_AUD	0 ~ 3.08	v
H3	AVSS18_AUD	0	v
G3	AVSS18N_AUD	-1.98 ~ 0	v
J1	AVSS28_AUD	0	v
F1	VBAT_SPK	0 ~ 4.5	v
D1	SPK_N	0 ~ 4.5	v
E1	SPK_P	0 ~ 4.5	v
F3	GND_SPK	0	v

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Ball	Symbol	Voltage range	Unit
J5	CLK26M	0 ~ 1.98	v
H2	HPL	-1.98 ~ 1.98	v
H1	HPR	-1.98 ~ 1.98	v
J2	HSN	-1.98 ~ 1.98	v
K2	HSP	-1.98 ~ 1.98	v
P16	AVSS22_XO	0	v
P17	AVSS22_XOBUF	0	v
R17	XTAL1	0~2.2	v
T17	XTAL2	0~2.2	v
N17	XO_SOC	0~1.21	v
L16	XO_WCN	0~1.98	v
M16	XO_CEL	0~1.98	v
N16	XO_NFC	0~1.21	v
L9	DCXO32K_EN	0~3.08	v
N9	XMODE	0~3.08	v
D12, D14, D6, D8, E10, E11, E12, E13, E6, E7, E8, E9, F10, F11, F12, F13, F6, F7, F8, F9, G10, G11, G12, G1, G6, G7, G8, G9, H10, H11, H12, H13, H14, H6, H7, H8, H9, J10, J11, J12, J13, J14, J15, J6, J7, J8, J9, K11, K12, K13, K14	GND_LDO	0	v

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2.4 Recommended Operating Range

Table 2-3. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Operating temperature range		-30		85	°C

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2.5 Electrical Characteristics

VBAT = 2.5V ~ 4.5V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation Ground Current					
Standby	Low-power mode		350	420	µA
Power down leakage current with 32K XTAL	VBAT=4.5V, Temp=25°C			85	uA
Power down leakage current without 32K XTAL (VTCXO24)	VBAT=4.5V, Temp=25°C			95	uA
Under Voltage (UV)					
Under voltage falling threshold		2.55	2.6	2.65	V
Threshold voltage accuracy		-50		+50	mV
Under voltage rising threshold (UVLO_VTHH) w/o charger	R=185K~270K	2.95	3.0	3.05	V
Under voltage rising threshold (UVLO_VTHH) w/i charger	R=185K~270K	2.75	2.8	2.85	V
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V
Output current (Ioh)	Vo > VIO-0.4V		1		mA
Delay time from VUSB33 turn on to RESETB release			42		ms
Interrupt					
Output high		VIO-0.4			V
Output low				0.2	V
PWRKEY/FCHR_ENB					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time			36		ms
Control Input Voltage					
Control input high (SPI, SRCLKEN related)		0.7*VIO			V
Control input low (SPI, SRCLKEN related)				0.3*VIO	V
Thermal Shut-down					
PMIC shut-down threshold			150		°C
Shut-down release threshold			110		°C

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2.6 Regulator Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VPROC					
Turn-on overshoot	Vout=1.0V No load			10	%
Short current		Imax*1.2		Imax*2.0	
Temperature coefficient	Vbat=3.8V I_Load=No Load	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.0V, L_DCR=30mΩ I_Load=100mA		83		%
	Vbat=3.8V, Vout=1.0V, L_DCR=30mΩ I_Load=500mA		79		%
	Vbat=3.8V, Vout=1.0V, L_DCR=30mΩ I_Load=1.0A		78		%
	Vbat=3.8V, Vout=1.0V, L_DCR=30mΩ I_Load=5A		60		%
Soft start	Vout=1.0V No load			200	us
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient (PWM)	Vbat=3.8V IOUT = 1.6A to 4.0A (slew rate=2A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.5V I_Load=10mA to Imax	-0.6		+0.6	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.1V to 4.5V I_Load=0~10mA	-3		+3	%
Buck – VCORE					
Turn-on overshoot	Vout=1.0V No load			10	%
Short current		Imax*1.2		Imax*2.0	
Temperature coefficient	Vbat=3.8V I_Load=No Load	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.0V, L_DCR=35mΩ I_Load=100mA		81		%
	Vbat=3.8V, Vout=1.0V, L_DCR=35mΩ I_Load=500mA		78		%
	Vbat=3.8V, Vout=1.0V, L_DCR=35mΩ I_Load=1.0A		75		%
	Vbat=3.8V, Vout=1.0V, L_DCR=35mΩ I_Load=3.5A		57		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
Soft start	Vout=1.0V No load~10mA			200	us
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient (PWM)	Vbat=3.8V IOUT = 1.2A to 3.5A (slew rate=2A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.5V I_Load=10mA to Imax	-0.6		+0.6	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.1V to 4.5V I_Load=0~10mA	-3		+3	%
Buck – VCORE2					
Turn-on overshoot	Vout=1.0V No load			10	%
Short current		Imax*1.2		Imax*2.0	
Temperature coefficient	Vbat=3.8V I_Load=No Load	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.0V, L_DCR=35mΩ I_Load=100mA		79		%
	Vbat=3.8V, Vout=1.0V, L_DCR=35mΩ I_Load=500mA		78		%
	Vbat=3.8V, Vout=1.0V, L_DCR=35mΩ I_Load=1.0A		75		%
	Vbat=3.8V, Vout=1.0V, L_DCR=35mΩ I_Load=3.5A		57		%
Soft start	Vout=1.0V No load~10mA			200	us
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient (PWM)	Vbat=3.8V IOUT = 1.2A to 3.5A (slew rate=2A/us)	-3.5		+3.5	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.5V I_Load=10mA to Imax	-0.6		+0.6	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.1V to 4.5V I_Load=0~10mA	-3		+3	%
Buck – VPA					
Turn-on overshoot	No load			10	%
Short current	a. Vo=0.5V~1.25V b.Vo=1.25V~3.4V		a. 0.8 b. 2		A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax/1.0*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.5V,		67		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	L_DCR<130mΩ R_Load=50 Ω				
	Vbat=3.8V, Vout=1.2V, L_DCR<130mΩ R_Load=15 Ω		80		%
	Vbat=3.8V, Vout=2.4V, L_DCR<130mΩ R_Load=13.3 Ω		89		%
	Vbat=3.8V, Vout=3.4V, L_DCR<130mΩ R_Load=12 Ω		92		%
Soft start	VBAT=3.8 ILOAD=50Ω Vo=0.5V/ 1.8V/ 3.4V		200		us
Output Ripple Voltage	a. PFM ripple @ VPA = 0.5V b. PFM ripple @ VPA > 0.5V c. PWM ripple @ 0.5V< VPA < 1.25V (Fsw=1Mhz) d. PWM ripple @ 1.25V<VPA < 3.4V (Fsw =2Mhz) e. PWM ripple @ 0.2V < VBAT-VPA < 1.0V 20MHz measurement BW			a.150 b.100 c.50 d.20 e. 180	mVp-p
Load transient	Vbat=3.8V,Vout=0.5V IOUT = 10mA~60mA, Tr/Tf = 5us Vo 22-36us average deviation with Vsettle			15	mV
	Vbat=3.8V,Vout=1.5V IOUT = 30mA~120mA, Tr/Tf = 1us Vo 22-36us average deviation with Vsettle			35	mV
	Vbat=3.8V,Vout=3.4V IOUT = 30mA~680mA, Tr/Tf = 1us Vo 22-36us average deviation with Vsettle			50	mV
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.5V I_Load=10mA to Imax	-5		+5	%
Buck – VS1					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax/ 1.0*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=2V, L_DCR=35mΩ I_Load=50mA		82		%
	Vbat=3.8V, Vout=2V, L_DCR=35mΩ I_Load=500mA		82		%
	Vbat=3.8V, Vout=2V,		75		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	L_DCR=35mΩ I_Load=1 A				
	Vbat=3.8V, Vout=2V L_DCR=35mΩ I_Load=1.9 A		62		%
Soft start	No load			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			1	%(mVpp)
Load transient	Vbat=3.8V IOUT = 0<–>250 mA. IOUT = 700mA<–>150 mA. IOUT = 800mA<–>1900mA (Tr/Tf=1uS)	-3.0		+3.0	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.1V to 4.5V I_Load=transient point to Imax	-1.0		+1.0	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.1 to 4.5V I_Load=0~ transient point	-1.0		+2.0	%

Table 2-6. LDO specifications

Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
All test conditions for input power range	ALDO and DLDO for VBAT range	(note#1) Min spec: max{Output Voltage +0.35V; VBAT≧3.1}		(note #1)		4.5	V
	SLDO1 for AVDD20 range	(note#2) Min spec: max{Output Voltage +0.15V; AVDD20≧2*0.99}		(note #2)		2*1.01	V
Overall DC voltage accuracy	VTCXO28,VXO22, VCN28,VCN18,VCAMA,VIO28,VIBR, VUSB33, VRF12	Iout= 0~0.8*Imax	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C	-5		+5	%
	Other LDOs			-2.5		+2.5	%
	Low power mode for ALDO, DLDO and SLDO	Iout= 0~0.05*Imax	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C	-5		+5	%
Load/Line regulation	Normal mode for ALDO, DLDO and SLDO	Iout= 0~Imax	1. Input power range 2. Typical capacitor 3. TA= 25°C	-1.5		+1.5	%
	VRTC and DVDD18_DIG	Iout= 0~0.25*Imax		-5		+5	%
	Low power mode for ALDO, DLDO and SLDO	Iout= 0~0.05*Imax		-5		+5	%
Power off voltage	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C 4. Iout= 0mA				0.1	V

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Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
Temperature coefficient	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C 4. Iout= 0 mA		-100		100	ppm/C
Load transient response	ALDO, DLDO and SLDO	Slew rate= 15mA/us	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C 4. Iout= 0.01*Imax~0.5*Imax	-5		+5	%
	VCN33, VSRAM_PROC, VDRAM, VMCH, VEMC, VIO18	Slew rate= 0.5*Imax/us		-4		+4	%
Turn-on rise time	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0mA		20		300	us
Turn-on overshoot	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0mA				Vout*1.1	V
Power off time	ALDO, DLDO and SLDO	Bypass capacitor ≦ 2.2uF	1. Input power range 2. TA= +25°C 3. Iout= 0mA			4	ms
		Bypass capacitor ≦ 4.7uF				8	ms
		Bypass capacitor ≦ 10uF				12	ms
Output noise	ALDO	Freq = 10Hz to 80kHz	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout=0.2*Imax ~0.5*Imax		90		uVrms
	DLDO and SLDO				500		uVrms
	ALDO, DLDO and SLDO	Freq = 10Hz to 10MHz			1000		uVrms
PSRR	ALDO	Freq = 217Hz to 3kHz	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0.2*Imax / 0.5*Imax		65		dB
		Freq= 3kHz to 30kHz			45		dB
	DLDO and SLDO	Freq = 217Hz			40		dB
Short current	VMCH, VEMC33	OC	1. Input power range 2. Typical capacitor 3. TA= +25°C	1.2 x Imax		2 x Imax	
	VXO22, VSIM1/2			2.4 x Imax		10 x Imax	
	ALDO, DLDO and SLDO	OC		1.2 x Imax		5 x Imax	
		OCFB		0.2 x Imax		2 x Imax	
Normal mode quiescent current	VCAMA, VSRAM_PROC, VDRAM, and VCAMD	1. Input power range 2.Typical capacitor 3. TA= +25°C 4. Iout= 0mA			300		uA

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Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
	VMCH, VEMC33, VIO28, VCN33			150		
	Other LDOs			55		
	VRTC28 and DVDD18_DIG			7		
Low power mode quiescent current	VSRAM_PROC, VMCH, VLDO28 and VEMC33			15		
	Other LDOs			10		

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2.7 Driver

Table 2-7. Driver specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
ISINK					
ISINK LED sink current	ISINK_SEL = 000		4		mA
	ISINK_SEL = 001		8		mA
	ISINK_SEL = 010		12		mA
	ISINK_SEL = 011		16		mA
	ISINK_SEL = 100		20		mA
	ISINK_SEL = 101		24		mA
ISINK dropout voltage	4 ~ 24mA VISINK drop			300	mV
ISINK rise/fall time	VISINK > 0.3V			3.33	uS
Pre-charge indicator					
LED sink current	VBUS=4.5~12V VBAT=2.2V~4.5V Visink=1.2V~2.8V		2		mA
			4		mA
			6 (default)		mA
Dropout voltage	VBAT=2.2V-4.5V 2mA~6mA Visink drop			1.2	V
Rise/Fall time	Visink>1.2V			3.33	uS
Breath mode two step rising/falling time	Two step corner rate		30		%
VIBR					
Output voltage	VIBR_SEL = 000		1.2		V
	VIBR_SEL = 001		1.3		V
	VIBR_SEL = 010		1.5		V
	VIBR_SEL = 011		1.8		V
	VIBR_SEL = 100		2.5		V
	VIBR_SEL = 101		2.8		V
	VIBR_SEL = 110		3.0		V
	VIBR_SEL = 111		3.3		V
Output current			200		mA

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2.8 Audio CODEC

Table 2-8. Class AB/D audio amplifier specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Class AB audio amplifier					
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		890		mW
	8Ω load, VBAT = 3.8V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		500		mW
	8Ω load, VBAT = 4.2V THD + N = 10%		1100		mW
	8Ω load, VBAT = 3.8V THD + N = 10%		850		mW
	8Ω load, VBAT = 3.4V THD + N = 10%		600		mW
THD+N	1kHz, Po = 0.5Wrms, VBAT = 4.2V		0.01	0.03	%
	1kHz, Po = 0.4Wrms, VBAT = 3.8V		0.01	0.03	%
	1kHz, Po = 0.3Wrms, VBAT = 3.4V		0.01	0.03	%
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 4.2V		80		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.4V		80		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
Noise level	VBAT = 4.2V, 12dB gain 8Ω, A-weighted		30		µV
	VBAT = 3.4V, 12dB gain 8Ω, A-weighted		30		uV
	VBAT = 4.2V, 0dB gain 8Ω, A-weighted		10		µV
	VBAT = 3.4V, 0dB gain 8Ω, A-weighted		10		uV
	VBAT = 4.2V, -6dB gain 8Ω, A-weighted		6		µV

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Parameter	Conditions	Min.	Typ.	Max.	Unit
	VBAT = 3.4V, -6dB gain 8Ω, A-weighted		6		uV
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load, VBAT=4.2V		5		mA
	No load, VBAT=3.8V		5		mA
	No load, VBAT=3.4V		5		mA
DC offset	VBAT = 4.2V, 12dB gain		5		mV
	VBAT = 3.8V, 12dB gain		5		mV
	VBAT = 3.4V, 12dB gain		5		mV
	VBAT = 4.2V, 0dB gain		1		mV
	VBAT = 3.8V, 0dB gain		1		mV
	VBAT = 3.4V, 0dB gain		1		mV
	VBAT = 4.2V, -6dB gain		1	5	mV
	VBAT = 3.8V, -6dB gain		1	5	mV
	VBAT = 3.4V, -6dB gain		1	5	mV
Class D audio amplifier					
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		900		mW
	8Ω load, VBAT = 3.8V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		500		mW
	8Ω load, VBAT = 4.2V THD + N = 10%		1100		mW
	8Ω load, VBAT = 3.8V THD + N = 10%		850		mW
	8Ω load, VBAT = 3.4V THD + N = 10%		600		mW
THD+N	1kHz, Po = 0.5Wrms, VBAT = 4.2V		0.02	0.16	%
	1kHz, Po = 0.4Wrms, VBAT = 3.8V		0.02	0.16	%
	1kHz, Po = 0.3Wrms, VBAT = 3.4V		0.02	0.16	%
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 4.2V		80		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.4V		80		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB

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Parameter	Conditions	Min.	Typ.	Max.	Unit
	20kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
Noise level	VBAT = 4.2V, 12dB gain 8Ω, A-weighted		60		µV
	VBAT = 3.4V, 12dB gain 8Ω, A-weighted		60		uV
	VBAT = 4.2V, 0dB gain 8Ω, A-weighted		25		µV
	VBAT = 3.4V, 0dB gain 8Ω, A-weighted		25		uV
Efficiency	VBAT = 4.2V 0.8W, 8Ω with 68uH, 1kHz		85		%
	VBAT = 4.2V 0.5W, 8Ω with 68uH, 1kHz		85		%
	VBAT = 3.8V 0.5W, 8Ω with 68uH, 1kHz		85		%
	VBAT = 3.4V 0.5W, 8Ω with 68uH, 1kHz		85		%
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load, VBAT=4.2V		5		mA
	No load, VBAT=3.8V		5		mA
	No load, VBAT=3.4V		5		mA
DC offset	VBAT = 4.2V, 12dB gain			5	mV
	VBAT = 3.8V, 12dB gain			5	mV
	VBAT = 3.4V, 12dB gain			5	mV
	VBAT = 4.2V, 0dB gain		1		mV
	VBAT = 3.8V, 0dB gain		1		mV
	VBAT = 3.4V, 0dB gain		1		mV

Table 2-9. Audio downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to audio buffer output (single-ended output, AU_HPL/R; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +0dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<0.1% THD		25		mW
SNR (1)	Signal to noise ratio (A-weighted)		100		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -86 -88 -86		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -84 -86 -84		dB
NF_{OUT}	Output noise floor (A-weighted)		4		µVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω

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Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
XT_{LR}	L/R channel crosstalk @1kHz		-90		dB
PSRR	Power supply rejection ratio (From AVDD18_AUD to AU_HPL/R)		90		dB
DAC to audio buffer output (single-ended output, AU_HPL/R; R_{LOAD} = 16) Temp = 25deg, 1kHz sinusoid signal, $Fs_{,DL}$ = 48kHz, Gain = +0dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<0.1% THD		35		mW
SNR (1)	Signal to noise ratio (A-weighted)		100		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -84 -88 -88		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -81 -86 -86		dB
NF_{OUT}	Output noise floor (A-weighted)		4		µVrms (A)

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to voice buffer output (differential outputs, AU_HSP/N; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $Fs_{,DL}$ = 48kHz, Gain = +0dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<1% THD		100		mW
SNR (1)	Signal to noise ratio (A-weighted)		104		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -87 -88		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -85 -86		dB
NF_{OUT}	Output noise floor (A-weighted)		5		µVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
PSRR	Power supply rejection ratio (From AVDD18_AUD to AU_HSP/N)		90		dB
DAC to voice buffer output (differential outputs, AU_HSP/N; R_{LOAD} =16) Temp = 25deg, 1kHz sinusoid signal, $Fs_{,DL}$ = 48kHz, Gain = +0dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<1% THD		130		mW
SNR (1)	Signal to noise ratio (A-weighted)		104		dB(A)

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Symbol	Parameter	Min.	Typ.	Max.	Unit
THD	Total harmonic distortion (THD) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -87 -88		dB
THD+N	THD Plus noise (THD+N) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -85 -86		dB
NF_{OUT}	Output noise floor (A-weighted)		5		μVrms (A)

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]

Table 2-10. Audio uplink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue input paths to ADC (differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		98		dB
N_{IN}	Input-referred noise		16		μVrms
THD	Total Harmonic Distortion (THD) @0dBV input (-3dBFS)		-89		dB
THD+N	THD plus noise (THD+N) @0dBV input (-3dBFS)		-86		dB
	THD plus noise (THD+N) @-60dBV input (-63dBFS)		-36		dB
Analogue input paths to ADC (differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		89		dB
N_{IN}	Input-referred noise		6.3		μVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-89		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-84		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-26		dB

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue input paths to ADC (differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		99		dB
N_{IN}	Input-referred noise		14		μVrms
THD	Total Harmonic Distortion (THD) @0dBV input (-3dBFS)		-87		dB
THD+N	THD plus noise (THD+N) @0dBV input (-3dBFS)		-85		dB
	THD plus noise (THD+N) @-60dBV input (-63dBFS)		-37		dB
Analogue Input Paths to ADC (differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, FS,UL = 48kHz, PGAUL gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		92		dB
N_{IN}	Input-referred noise		4.2		μVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-87		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-84		dB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-29		dB

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured w/i A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Note 2: The input voltage range of AU_VIN0, AU_VIN1, and AU_VIN2 are within [AVDD28_AUD, AVSS28_AUD], and suggesting maximum input swing $V_{pp} \leq 1V_{rms}$ (0 dBV) @ PGA_{UL} gain = 0dB

General					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
$APGR_{UL}$	Uplink analog programmable gain range	0		24	dB
$APGS_{UL}$	Uplink analog programmable gain step		6		dB
CMRR	Common-mode rejection ratio @-18dBV, 1kHz sinusoid signal to both pins of an input configured differentially	40	76		dB
$XT_{Internal}$	ULL-to-ULR channel separation @ one input terminated with -18dBV, 1kHz sinusoid signal. Measure digital output of terminated channel	60	100		dB
XT_{DL2UL}	DL-to-UL channel separation @ 0dBV, 1kHz Rx path with RLOAD = 32	60	101		dB
PSRR	217Hz @ 200 mVpp square wave imposed on power. Measure digital output		-70		dB
	1kHz @ 200 mVpp square wave imposed on power. Measure digital output		-70		dB
	10kHz @ 200 mVpp square wave imposed on power. Measure digital output		-70		dB
$F_{S,UL}$	Audio uplink sampling rate 8, 16, 32, and 48kHz	8		48	KHz

Digital MIC					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
DCLK	DMIC clock frequency		3.25/1.62		MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time (MaxCL = 65p)			10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)			10	ns

Table 2-11. MICBIAS specifications

Microphone Bias (MICBIAS) Temp = 25deg, 1µF capacitor on MICBIAS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OUT}	Microphone bias voltage	1.7		2.5	V
V_{OUT} Step	Bias voltage output step size 1.7~2.1 2.3~2.5		0.1		V
I_{OUT}	Maximum output current (two MICBIAS loads total)			3	mA
N_{OUT}	Output integrated noise (20~20kHz A-weighted) with 1µF cap.		3.9		µVrms
PSRR	217Hz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		-100		dB
	1kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		-100		dB

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Microphone Bias (MICBIAS) Temp = 25deg, 1μF capacitor on MICBIAS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
	10kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		-95		dB
$C_{LOAD,MIC}$	Output capacitor load on MICBIAS	0.1		22	μF

Table 2-12. ACCDET specifications

Accessory Detection (ACCDET)					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
-	*1: Load impedance detection range (ACCDET) by 1& 1.5kΩ (1%) MICBIAS resistors *2: Note the characteristics assume no other component is connected to ACCDET *3: Note the key detection voltage will be normalized automatic. For different MICBIAS setting , the same key (resistance is the same)is pressed , read voltage (key pressed) value will be similar				
-	4 pole microphone detection	2K		14K	Ω
-	Microphone impedance detection after 4-pole microphone plugged-in				
-	MICD_LVL[0]: Down key	400		620	Ω
-	MICD_LVL[1]: Up key	150		320	Ω
	MICD_LVL[2]: Hook key	0		100	Ω

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2.9 Battery Charger

Table 2-13. Charger specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
CHRIN operating voltage		4.3	5	10.5	V
OTG B-Valid detection		0.8	2.4	4	V
VCDT detection threshold	VCDT_VTHL[3:0] = 0000 ~ 1111	4.3		10.5	V
HV adaptive current @ pre_charge	CHRIN switch threshold (300mA => 70mA)		7		V
	CHRIN switch threshold (70mA => 300mA)		6		V
VBAT CC voltage accuracy	Programmable: 3.3~3.45, 50mV steps	-70		+70	mV
VBAT CV voltage accuracy	Programmable: 3.5~4.4 V	-30		+30	mV
VBAT OV voltage accuracy	Programmable: 3.9~4.5 V	-30		+30	mV
CC mode charging current accuracy	Programmable:500 ~2000 mA (Rsense=56mΩ)	-10		+10	%

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2.10 BC1.x

Table 2-13. BC1.x specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
BC11 charging port detection (Pre-CC current)	Standard down-stream port		70		mA
	Standard charging down-stream port		70		mA
	DP, DM short		300		mA
BC11 characteristics	DP, DM floating		300		mA
	IPU_DP, IPU_DM	7	9.6	13	uA
	IPD_DP, IPD_DM	50	96	150	uA
	VSRC on DP, DM	500	630	700	mV
	Current pulse value under 2.2V		70		mA
	Current pulse period under 2.2V		550		ms
	OSC1M, timer		5		min

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2.11 Down Load Without Battery

Table 2-14. Download without batteryspecifications

Parameter	Conditions	Min.	Typical	Max.	Unit
USBDL	Duration		32.0		s
	Current		450		mA

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2.12 AUXADC

Table 2-15. AUXADC specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply voltage		-	1.8	-	V
Resolution	Channel 0,1,7	-	-	15	Bits
	Others	-	-	12	Bits
Analog-input bandwidth			50K		Hz
Sample rate			100K		Hz
Offset error	Relative to full-scale	-1	-	+1	%
Gain error	Relative to full-scale	-1	-	+1	%
INL	15-bit output		2		LSB
DNL	15-bit output		2		LSB

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2.13 Fuel Gauge

Table 2-16. Fuel gauge specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
FG current characteristics	Output resolution		16		Bit
	Conversion time		1/16		s
	Over-sampling ratio	2^11		2^18	
ADC characteristics	Input voltage range	-60		60	mV
	Supply		2.8		V
	Current		40		uA
	Gain error	-2		2	%
	Accuracy		0.03		%

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2.14 DCXO

Table 2-17. XO specification

Parameter	Condition	Title	Unit	Min.	Typ.	Max.
Supply current in suspend (OSC LPM)	VXO22=2.2V; without 32K RTC	$I_{xo,lpm}$	uA		50	
Supply current in idle (OSC + one buffer for SOC)	VXO22=2.2V; PCB Cload<20pF	$I_{xo,idle}$	mA		2	
Supply current in RF TRx (OSC + buffers for SOC, RF_Cell)	VXO22=2.2V; PCB Cload<20pF	$I_{xo,trx}$	mA		4	
Extra supply current for RF_Conn	VXO22=2.2V; PCB Cload<20pF	$I_{xo,conn}$	mA		2	
Extra Supply current for RF_NFC	VXO22=2.2V; PCB Cload<20pF	$I_{xo,nfc}$	mA		1	
Leakage current	VXO22=2.2V; with 32K RTC	$I_{xo,leak}$	uA			1
Center operating frequency	Internal resonant; with QVL crystal	F_{dcxo}	MHz		26	
Duty cycle	Square wave in high driving mode		%	45	50	55
Static tuning range	XTAL1/2 differential input capacitance	C_{TR}	pF	4.0		8.5
CapID binary bits	CDAC		bit		8	
Startup time, after clock request	Delta f < 1ppm.	$T_{startup}$	ms		1	2
Crystal input pins	Specific foundries		pin		2	
Crystal size	CL=7~7.5pF			2016	2520	3225

Table 2-18. Reference input buffer specification (XTAL1, buffer mode)

Parameter	Conditions	Min.	Nom.	Max.	Unit
Input Impedance – Rp	Rp || Cp @ 26MHz	3	5		kΩ
Input Impedance – Cp	Rp || Cp @ 26MHz		5	10	pF

This pin should be AC coupled when used with an external clock source.

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2.15 Type-C

Parameter	Conditions	Min.	Typical	Max.	Unit
R_Pull Down	VUSB>2.93V	-10%	5.1K	10%	Ω
R_Pull Down	VUSB<2.93V, CC pin voltage > 1V	-20%	5.1K	20%	Ω
I_Pull up	VUSB>2.93V	-20%	80	20%	uA
I_Pull up	VUSB>2.93V	-8%	180	8%	uA
I_Pull up	VUSB>2.93V	-8%	330	8%	uA
zOPEN	VUSB>2.93V ,Minimum Impedance to GND	126k			Ω
CC detection threshold	Default USB Power	0.16	0.2	0.24	V
CC detection threshold	USB Type-C Current @3 A	0.61	0.68	0.7	V
CC detection threshold	USB Type-C Current @ 1.5 A	1.16	1.28	1.31	V
Threshold (UFP attach VTH and INT out)		0.16	0.2	0.24	V
Threshold (DFP attach VTH and INT out)		2.58	2.6	2.62	V
Standby current	DRP(50%)			12	uA
USB33_RDY_V43 power good	Power good for Type C block(Vbat rising)	2.88	2.93	2.98	V
	Power good for Type C block(Vbat falling)	2.8	2.85	2.9	V

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3 Functional Descriptions

3.1 General Descriptions

MT6353 is a fully integrated PMIC target for smart phone power provider. The following is the block diagram of MT6353 PMIC.

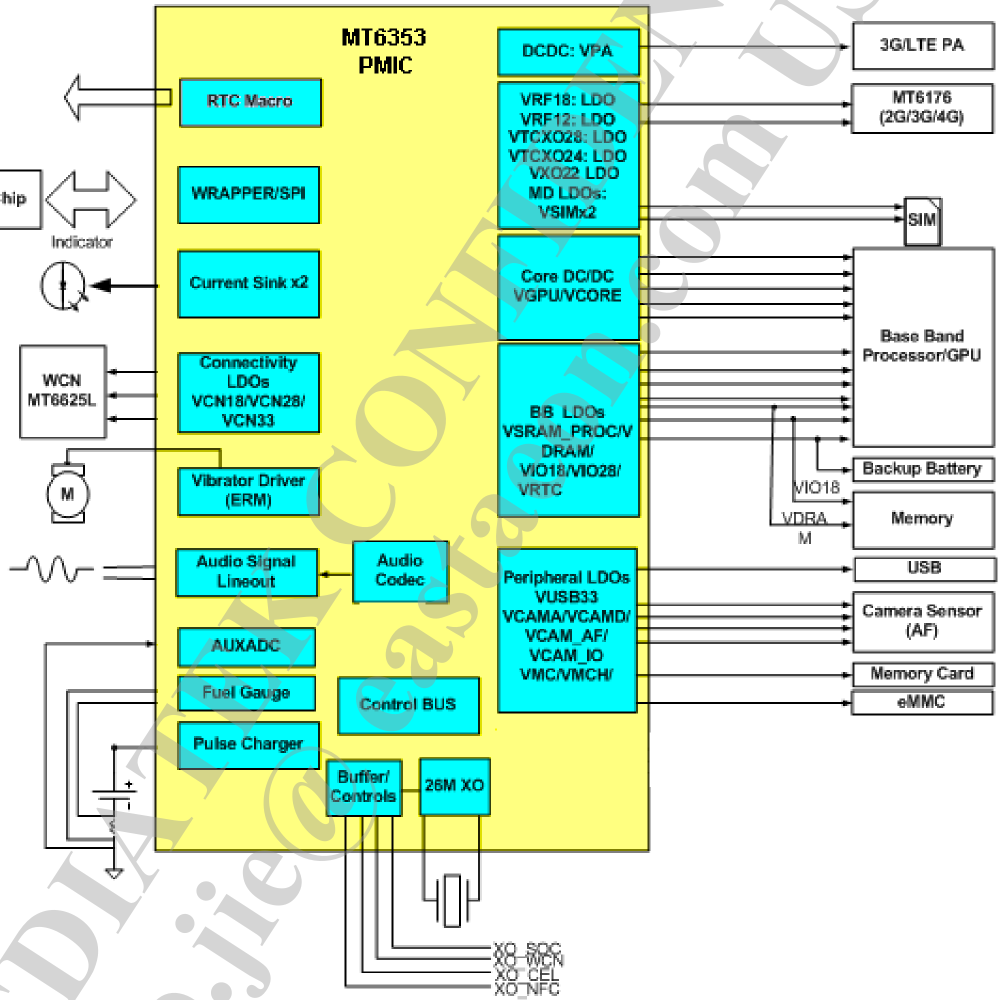

Figure 3-1. MT6353 block diagram

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3.2 PMIC Functional Blocks

MT6353 manages the power supply of baseband processor, SIM cards, camera, vibrator, etc. MT6353 includes the following analog functions for use on smart phone platforms.

- LDO and BUCK: Provides regulated lower output voltage level from Li-Ion battery
- Current sink (ISINK) driver: Sink current for indicator
- Vibrator driver: Provides regulated power for vibrator.
- AUXADC: 15 bits of analog to digital converter for thermal/accessory detection monitor and measurement
- Controller: Generates power-on/off sequence, system reset and exceptional handling function
- Charger controller: Controls/Protects battery charging procedure
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are explained in the following sections.

3.2.1 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ UVLO_VTHH) nor in the thermal condition, there are two methods to power on the handset system.

1) Pulling PWRKEY low (User presses PWRKEY.)
2) Valid charger plug-in

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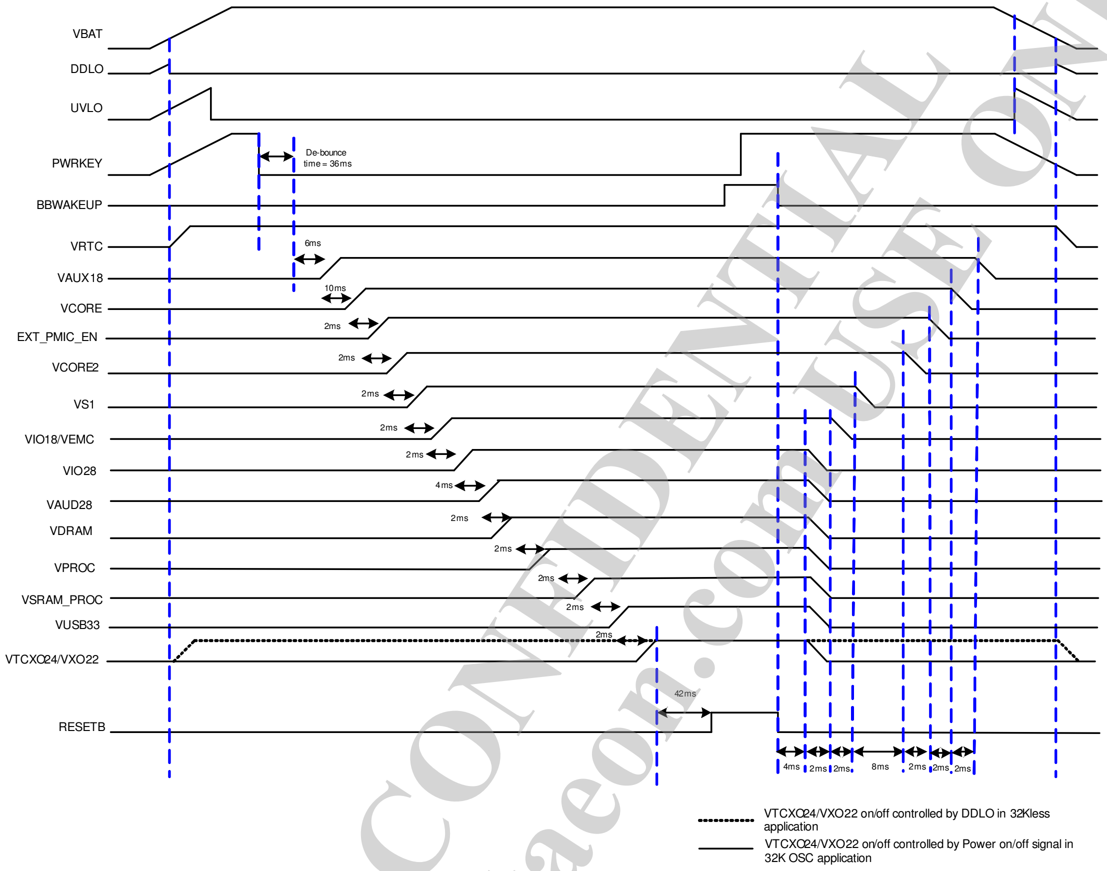

Figure 3-2. Power-on/off control sequence with XTAL by pressing PWRKEY

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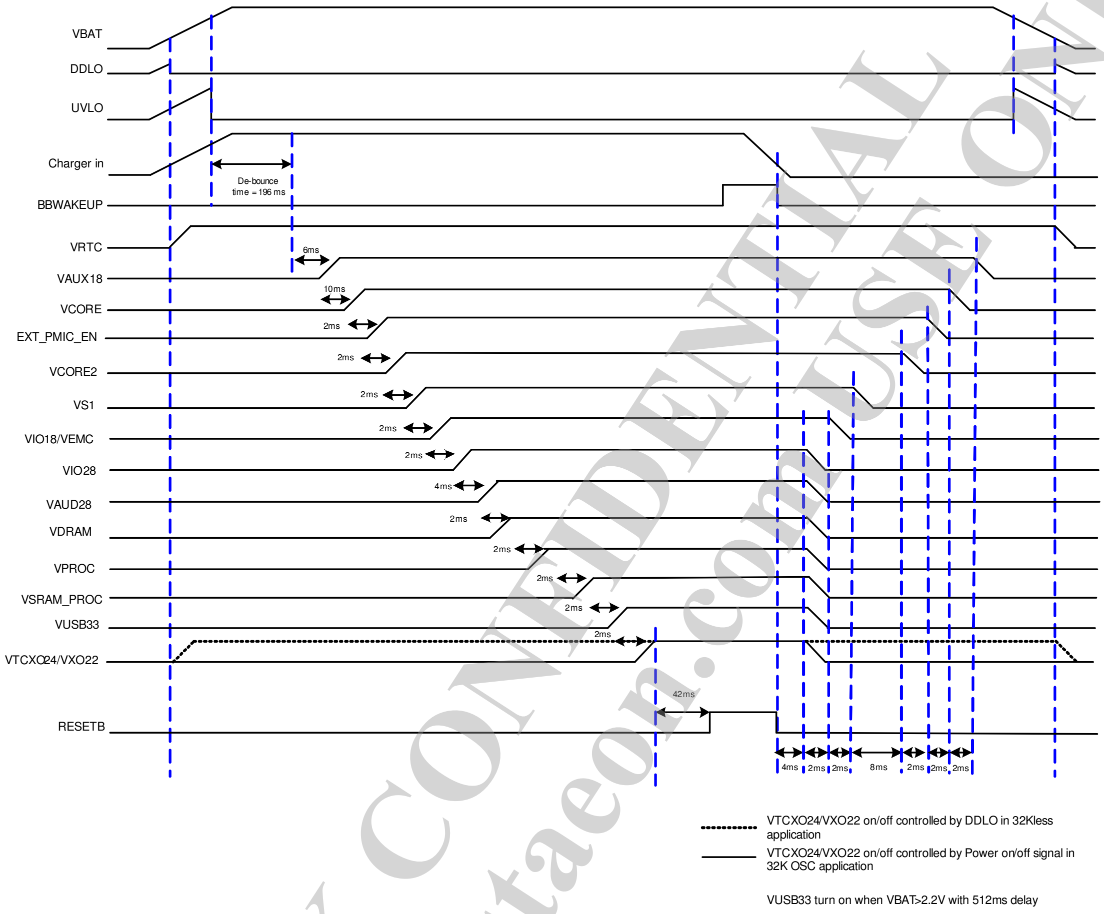

Figure 3-3. Power-on/off control sequence with XTAL by charger plug in

1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the BBWAKEUP signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives BBWAKEUP from the baseband.

2. RTC module generates BBWAKEUP to wake up the system.
   If the RTC module is scheduled to wake up the handset at some time, the BBWAKEUP signal will be directly sent to PMIC. In this case, BBWAKEUP becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid. When CHRIN input voltage> CHRIN_LV_VTH and V_{BATSYS}>UVLO, the handset will also be powered on.

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Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by BATSNS. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)

PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset

PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Buck Converter and Application Reference

There are five buck converters in MT6353 to efficiently generate regulated power for graphic processor, digital core and circuits. The block diagram is shown in Figure 3-1. The buck converters operate with 3 or 2MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters Pulse Frequency Modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal Over-Current Protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

Table 3-1. Buck converter brief specifications

BUCK name	Default voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VCORE	0.9	0.6 ~ 1.31	6.25	3,000	Y	Digital core always
VCORE2	1	0.6 ~ 1.31	6.25	3,500	Y	MODEM
VPROC	1	0.6 ~ 1.31	6.25	5,000	Y	PROCESSOR

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BUCK name	Default voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VS1	2	1.95 ~ 2.20	12.5	1,900	Y	SYS LDOs power
VPA	0.5	0.5~3.4	50	800	N	3G/LTE PA

3.2.3 Low Dropout Regulator (LDOs) and Application Reference

Table 3-2. LDO types and brief specifications

Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
ALDO	VTCXO28	VBAT_LDO1	2.8	2.8	40mA	N	RFFE
ALDO	VTCXO24	VBAT_LDO2	2.375	2.375	40mA	Y	DCXO
ALDO	VXO22	VBAT_LDO2	2.2	2.2	20mA	Y	DCXO
SLDO	VRF18	AVDD20_LDO5	1.825	1.825	400mA	N	RF
SLDO	VRF12	AVDD20_LDO5	1.2	1.2	150mA	N	RF
DLDO	VCN33	VBAT_LDO2	3.3	3.3/3.4/3.5/3.6	350mA	N	WCN
ALDO	VCN28	VBAT_LDO1	2.8	2.8	40mA	N	WCN
SLDO	VCN18	AVDD20_LDO2	1.8	1.8	150mA	N	WCN
ALDO	VCAMA	VBAT_LDO1	2.8	2.5/ 2.8	200mA	N	CAMERA
SLDO	VCAMIO	AVDD20_LDO2	1.8	1.8	200mA	N	CAMERA
SLDO	VCAMD	AVDD20_LDO2	1.3	0.9/1.0/1.1/1.22/1.3/1.5/1.8	<=1.5V: 500mA 1.8V: 300mA	N	CAMERA
ALDO	VAUX18	VBAT_LDO1	1.8	1.8	40mA	Y	AuxADC
ALDO	VAUD28	VBAT_LDO1	2.8	2.8	40mA	Y	Audio
SLDO	VSRAM_PROC	AVDD20_LDO4	1.1	0.6~1.31	400mA	Y	SRAM_PROC
SLDO	VDRAM	AVDD20_LDO1	1.24	1.24	1,000mA	Y	DRAM
DLDO	VSIM1	VBAT_LDO4	1.8	1.7/1.8/1.86/2.76/3.0/3.1	50mA	N	SIM1 card
DLDO	VSIM2	VBAT_LDO4	1.8	1.7/1.8/1.86/2.76/3.0/3.1	50mA	N	SIM2 card
DLDO	VLDO28	VBAT_LDO4	2.8	2.8	300mA	N	Touch Panel and CAMERA_AF
DLDO	VIO28	VBAT_LDO4	2.8	2.8	200mA	Y	IO and Sensor
DLDO	VMC	VBAT_LDO5	3	1.8/2.9/3.0/3.3	200mA	N	MSDC

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Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
DLDO	VMCH	VBAT_LDO5	3	2.9/3.0/3.3	800mA	N	SD Card
DLDO	VEMC33	VBAT_LDO3	3	2.9/3.0/3.3	800mA	Y	EMMC and UFS
DLDO	VIBR	VBAT_LDO4	2.8	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200mA	N	Vibrator
DLDO	VUSB33	VBAT_LDO2	3.3	3.3	50mA	Y	USB
SLDO	VIO18	AVDD20_LDO3	1.8	1.8	600mA	Y	IO and EMMC
VRTC28	VRTC28	VBAT_LDO1	2.8	2.8	2mA	Y	RTC macro
VDIG18	DVDD18_DIG	VBAT_LDO2	1.8	1.8	20mA	Y	PMIC digital
Power Switch	TREF	VBAT_LDO1	1.8	1.8	1mA	N	Battery Interface

3.2.4 Drivers

MT6353 supports two indicator LED drivers at most. The following figure depicts the major application for indicator LEDs drivers. LED driver of MT6353 supports PWM mode and Breath mode.

When the LED current is from small to large then descends,it is the breath mode.

Through software programming the registers in Figure 3-5, MT6353 can change the breathing cycle time, including Trising_1, Trising_2, Ton, Toff, Tfalling_1 and Tfalling_2 period.

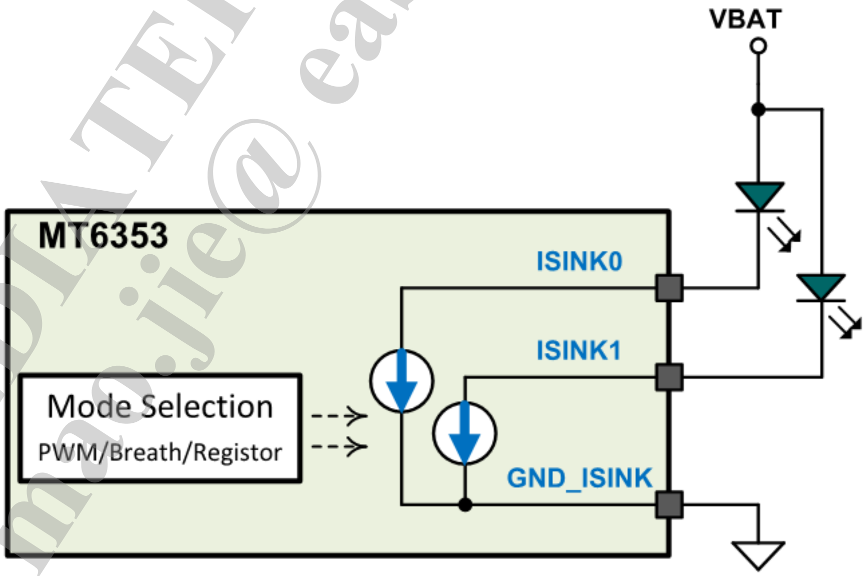

Figure 3-4. Configuration for indicator LED drivers

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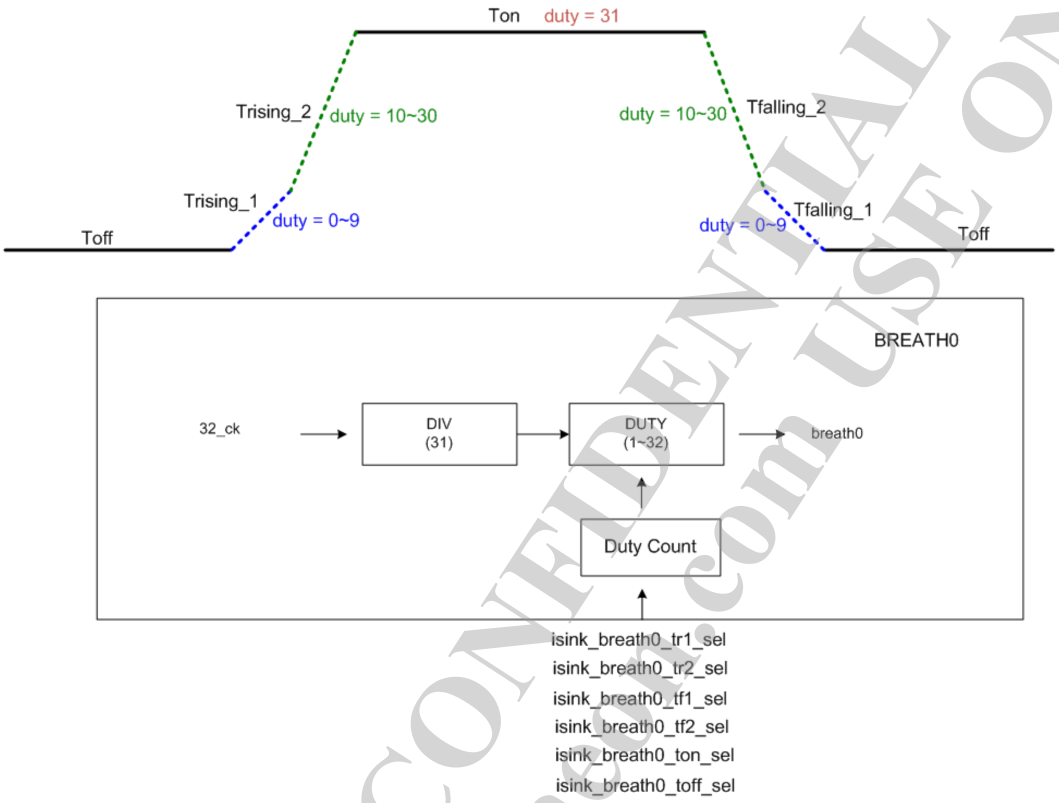

Figure 3-5. LED drivers breath mode

3.2.5 Pre-Charge Indicator

MT6353 supports an indepentdent indicator LED driver (pre-charge indicator). Once the charger is plugged in, the indicator will be always on to indicate the system is being charged. After the software works with the existing charger, it will have the same function as other LED drivers do.

3.2.6 Vibrator Driver

The VIBR driver power allows up to 200mA current for ERM (Eccentric Rotating Mass) or coin type vibrator with programmable output voltage.

3.2.7 Audio CODEC and Accessory Detection

3.2.7.1 Block Descriptions

The block diagram of audio codec is illustrated below. The audio uplink path is composed of PGA and audio ADC. There are three input pairs of the uplink path to support dual-MIC, earphone-MIC, and

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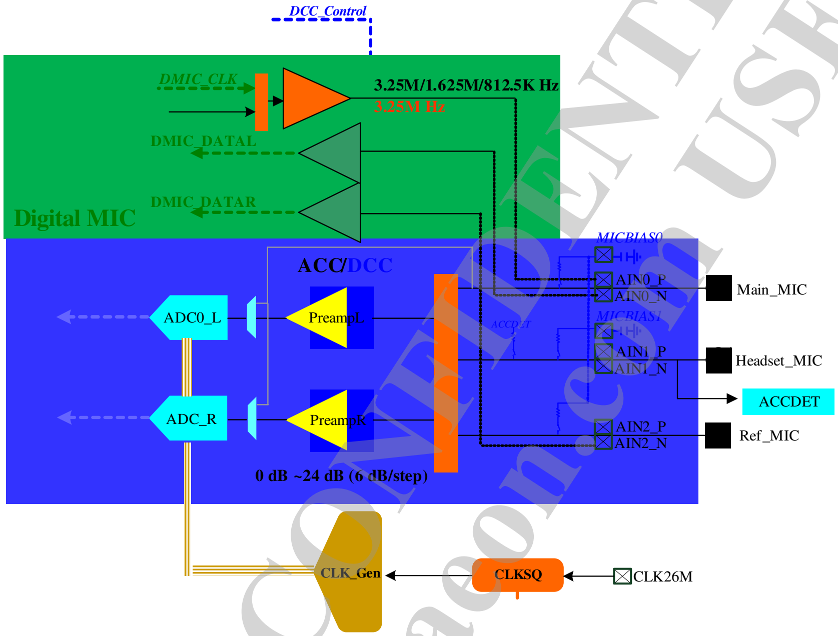
digital MIC. The uplink front-end to PGA can be configured as ACC or DCC type. The audio downlink is composed of stereo audio DACs, stereo headphone drivers and a mono voice driver. High-fidelity audio is reproduced on headphones and clear mobile speech on earpiece is driven by voice drivers. The internal high output power loud-speaker amplifier is also embedded. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec.



(a) Audio/speech uplink and accessory detection

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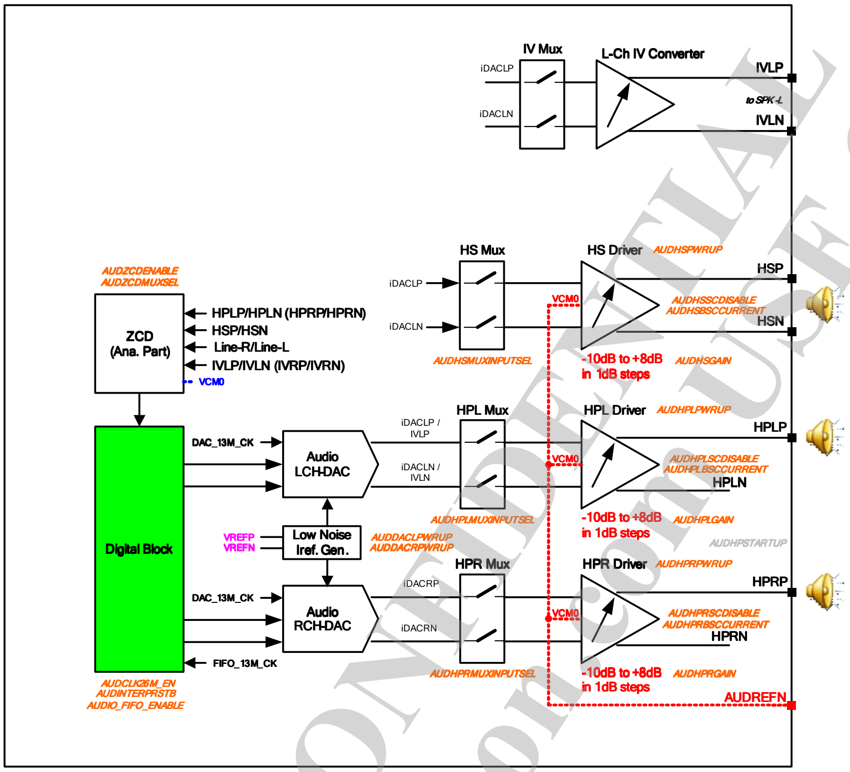

(b) Audio/speech downlink

Figure 3-6. Audio CODEC block diagram

3.2.8 Class-AB/D Audio Amplifier

MT6353 has one built-in channel high efficiency class AB/D audio power amplifier capable of delivering 0.7 watt of power on an 8 Ω BTL load from a 3.7V battery supply. Over-current protection is integrated. MT6353 also has built-in receiver mode for 2-in-1 loudspeaker which supports multi-purpose loudspeaker without any extra BOM cost. The output power can reach 97mW onto 8 Ω speaker load. The block diagram is shown below.

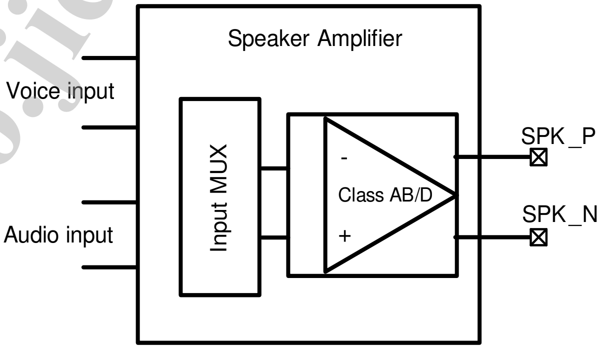

Figure 3-7. Block diagram of class-AB/D

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3.2.9 Battery Charger (Charger Controller)

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector resists higher input voltages than other parts of PMIC.

3.2.9.1 Block Descriptions

The block diagram of battery charger is illustrated below.

Charger block diagram

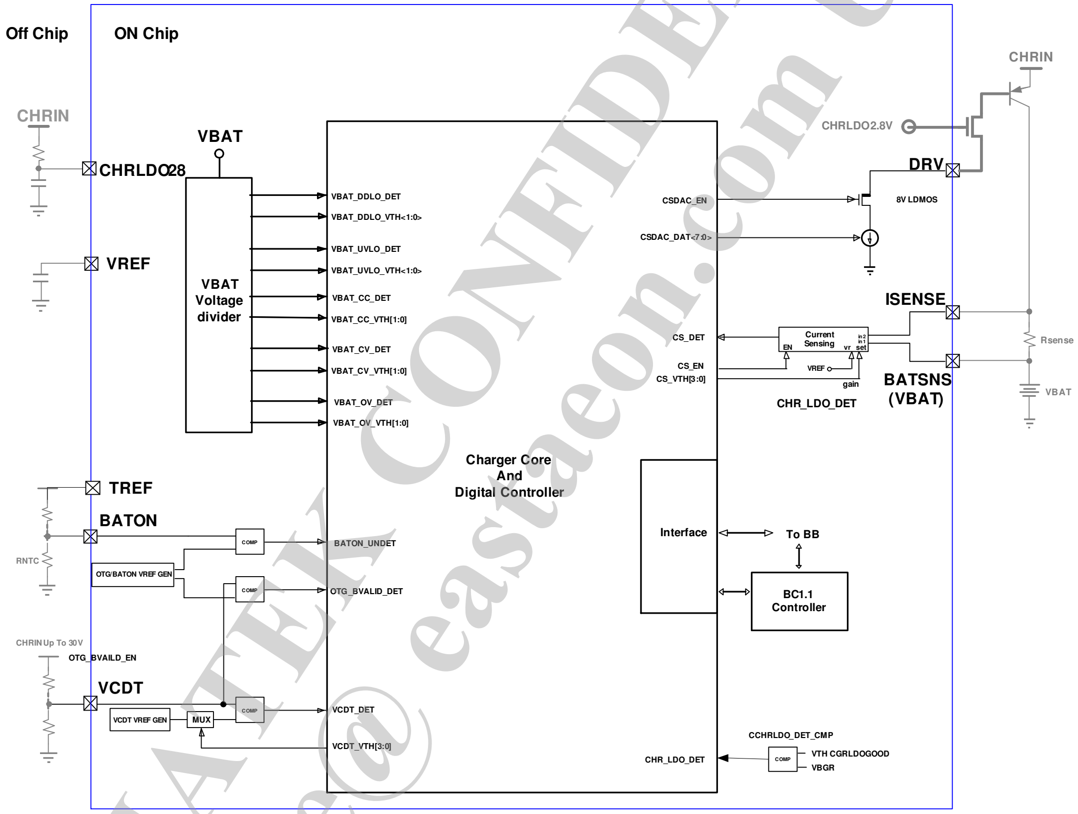

Figure 3-8. Block diagram of battery charger

3.2.9.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0V, software default setting), the charger detector will stop the charging process immediately to avoid burning out the chip or even the phone. Furthermore, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

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3.2.9.1.2 Charging Control

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.0V, PMIC power-off state), CC mode (Constant Current mode or fast charging mode at the range of 3.0V < VBAT < 4.2V, CV default voltage) and CV mode (Constant Voltage mode) to optimize the charging procedure for Li-ion battery. See the figure below for the charging states diagram.

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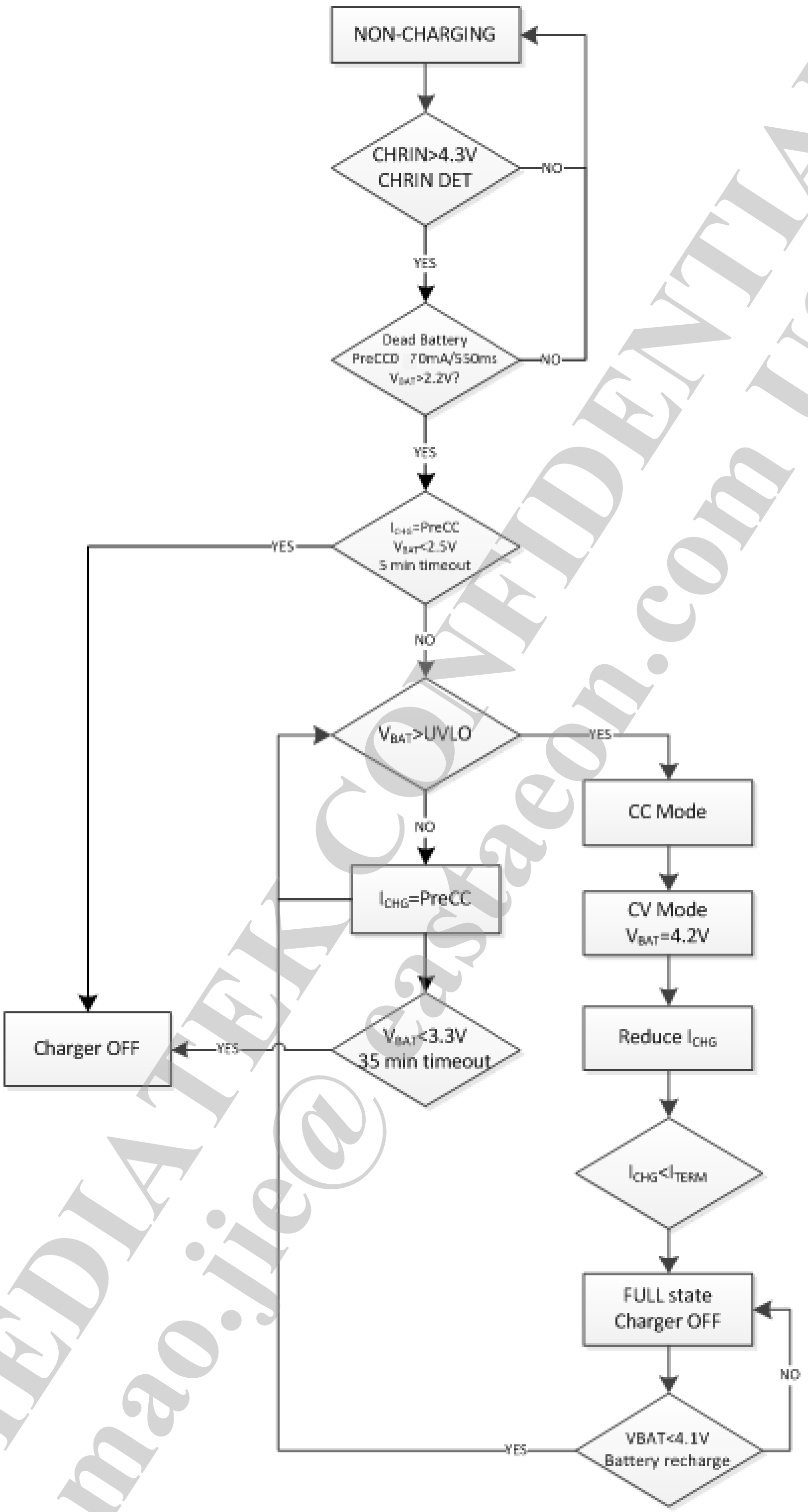

Figure 3-9. Flow chart of charging states

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Pre-charge mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, IUNIT trickle charging current is applied to the battery.

The IUNIT trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, i.e. the PRECC1 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external RSENSE is kept around 16.8mV (AC charger) or 3.92mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC1,AC adapter} = \frac{V_{SENSE}}{Rsense} = \frac{16.8mV}{Rsense}$$

$$I_{PRECC1,USB HOST} = \frac{V_{SENSE}}{Rsense} = \frac{3.92mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.0V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.056Ω, the CC mode charging current can be set from 70mA to 2,000mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant-voltage mode and over-voltage protection (OV)

When the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. When the battery voltage actually reaches 4.2V, the charging current gradually decreased step-by-step, and the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches termination current automatically and this mechanism is optimized for different battery packs. Whenever the battery voltage exceeds 4.3V (programmed by SW), a hardware OV protection will be activated and turns off the charger immediately.

3.2.9.1.3 BC1.x Dead-Battery Support

MT6353 also supports dead-battery condition BC1.x. These specifications protect dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after the trickle current is applied, the charger will be disabled. On the other hand, once the battery voltage rises to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be 70mA or 300mA depending on the type of the charging port.

When the battery is below 3.0V, the charger will charge the battery by the PRECC1 current.

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A dedicated 5 min. (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.4V under charging. Another 35 min. (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.0V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

3.2.9.1.4 Auto Power-On Mode (USB Download without Battery)

MT6353 features a default auto power-on mode (or USB DL without battery) no matter with or without battery. You can disable auto power-on by adding external pull-high resistor on the FCHR_ENB pin. USB DL (auto power-on) can still be initiated by pressing DL_KEY or under valid BAT_ON information (decided by customers' PCB options). Nonetheless, DL_KEY supports key function in normal mode. The valid BAT_ON information can be detected through the battery's NTC when it is connected to pin BAT_ON of MT6353.

3.2.10 AUXADC

3.2.10.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the input channels. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data..

Table 3-3. Application and input range of ADC channels

Channel	Application	Input range [V]
0	BATSNS	2.5 ~ 4.5
1	ISENSE	2.5 ~ 4.5
2	VCDT	0 ~ 1.5
3	BATON	0.1 ~ 1.7
5	ACCDET	0 ~ 1.8
6	TYPE-C	0 ~ 1.8
7	AUXADC_VIN	0 ~ 1.8
others	Internal use	N/A

3.2.11 Fuel Gauge

The fuel gauging system includes a dedicated ADC for Li-Ion battery current measurement and utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the three measuring methods and the accumulated current measurement. The application diagram of the fuel gauging

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system is shown in the figure below, where an external resistor is used to convert the current drawn from the battery into a voltage which is then measured by FG ADC. The value of the external resistor must be chosen so that the maximum current during charging or discharging will not cause ADC to exceed its input voltage range.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting. The hardware also includes necessary modes to allow for simultaneous current and voltage measurement which can be utilized to estimate the battery impedance.

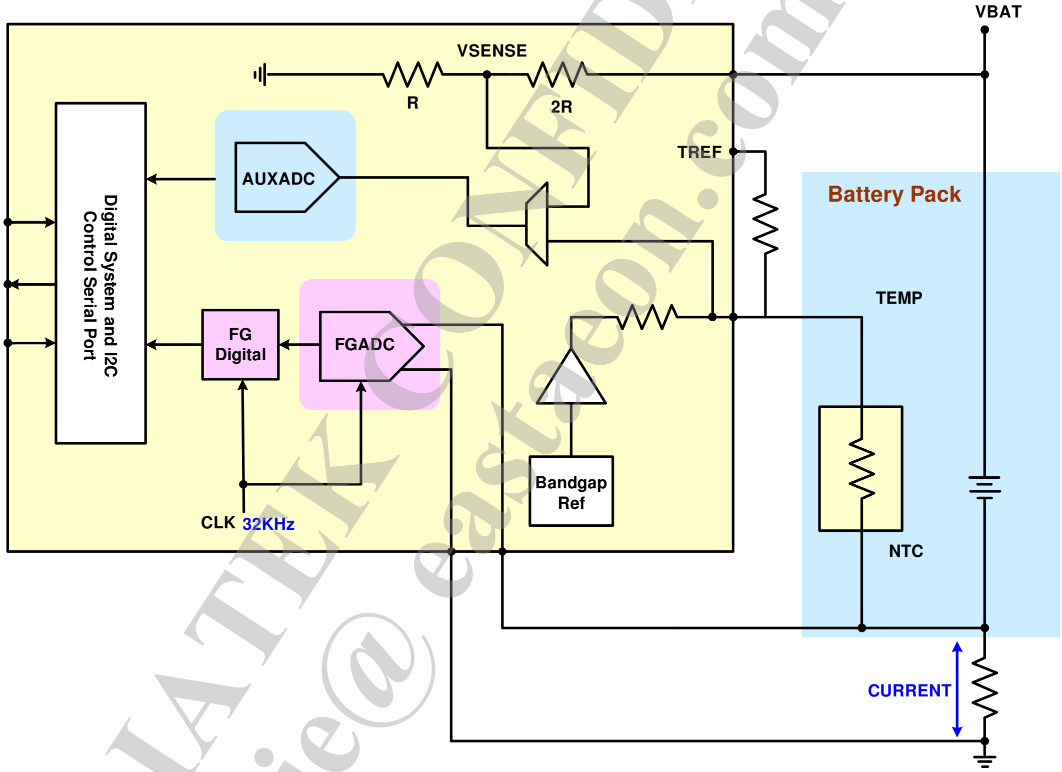

Figure 3-10. Fuel gauge block diagram and external connection

3.2.12 Real-time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin.

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Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

In MT6353, RTC module also supports function without 32kHz crystal. It can be configured by hardware option. The two configurations are shown below. While crystal is absent, RTC module has an embedded 32kHz oscillator to assist life time extension after master 32kHz clock is off.

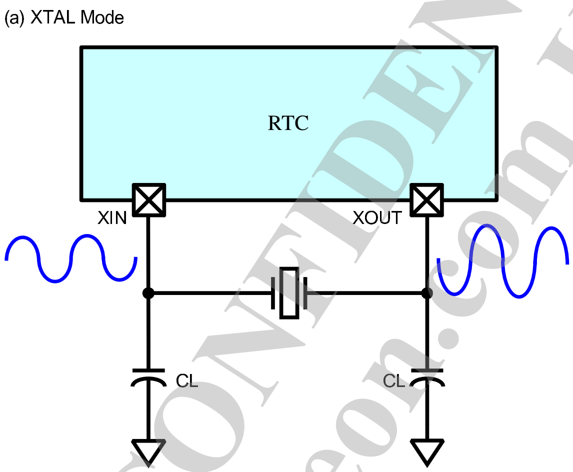

Figure 3-11. RTC configuration methods for XTAL

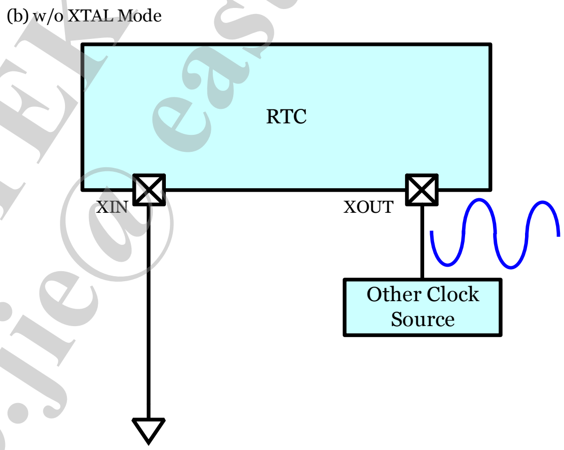

Figure 3-12. RTC configuration methods for w/o XTAL mode

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3.2.12.1 32kHz Crystal Oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. The key performance is shown in the table below.

Table 3-4. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power	1.1	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	20		80	%
I	Current consumption		5		µA
T	Operating temperature	-20		80	˚C

The minimum VRTC value means if the crystal oscillator starts up successfully, the minimum VRTC for the clock to still be alive is 1.1V.

Since the crystal parameters determine the oscillation allowance, see below for a few recommendations for the crystal parameters to be used well with XOSC32 in MT6353.

Table 3-5. Recommended parameters of 32kHz crystal

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level	0.5			uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	KΩ
Co	Static capacitance		0.9	2	pF
CL[1]	Load capacitance	6		12.5	pF

Under such CL range and crystal, the –R is greater than three times. If the CL selected is larger, the frequency accuracy will be decreased, and the –R will also degrade.

3.2.13 DCXO

3.2.13.1 Reference Clock Specification

MT6353 PMIC integrates a core 26MHz XTAL oscillator (XO) and supports 32kHz RTC-removal low power mode. It also provides backward compatible (BCM) configurations for previous solutions. There are two High Performance (1.8V_{PP}) and two Low Power (1.0V_{PP}) external clock buffers for the entire system and one internal buffer for audio.

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The modes of operation are configured by two input pins, DCXO32K_EN and XMODE, and the definitions are shown as below.

DCXO32K_EN	XMODE	Mode
LOW	LOW	Buffer mode with external TCXO
LOW	HIGH	Oscillator mode with 32K RTC
HIGH	LOW	BC M mode, system clock from RF
HIGH	HIGH	Oscillator mode without 32K RTC

In oscillator mode, the Temperature Sensing Crystal (TSX) is connected between XTAL1 and XTAL2. In buffer mode, the external clock inputs from XTAL1. Keep XTAL2 pin NC.

Note that the logic of DCXO32K_EN and XMODE must be directly shorted to GND or VRTC28 so that MT6353 can select proper power-on-sequence for different system configurations.

3.2.13.2 Reference Output Buffer(s) Specification

There are four 26MHz clock output buffers driving out from the chip. They can be used as reference clocks for other chips and applications. Two High Performance (HP) external buffers output 0~1.8V squarer wave, and two Low Power (LP) external buffers output 0~1.0V squarer wave. Note that all their DC common mode voltage is not zero, so DC block capacitor is required if it is AC coupled and specific common mode voltage.

The current of all buffers can be optimized for different PCB Cloading. Typical current consumption is optimized for < 20pF Cloading.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Zload (Rp||Cp)	Rp	3			kΩ
	Cp			30	pF
Duty cycle		40		60	%
Rise/Fall time	10% to 90% of signal swing @ Cload=30pF			5	ns
HP buffer output	Square wave	1.6	1.8	2.0	Vp-p
HP SSB phase noise	1Hz offset [30pF load]			-50	dBc/Hz
	5Hz offset [30pF load]			-73	dBc/Hz
	10Hz offset [30pF load]			-80	dBc/Hz
	100Hz offset [30pF load]			-106	dBc/Hz
	1kHz offset [30pF load]			-134	dBc/Hz
	10kHz offset [30pF load]			-144	dBc/Hz
	100KHz offset [30pF load]			-152	dBc/Hz
HP current consumption	Zload = 20pF (each buffer)		2.2		mA
LP buffer output	Square wave	0.8	1.0	1.2	Vp-p
LP SSB phase noise	100Hz offset [30pF load]			-85	dBc/Hz
	1kHz offset [30pF load]			-110	dBc/Hz
	10kHz offset [30pF load]			-130	dBc/Hz

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Parameter	Conditions	Min.	Nom.	Max.	Unit
	100kHz offset [30pF load]			-130	dBc/Hz
LP current consumption	Zload = 20pF (each buffer)		1.0		mA

3.2.13.3 32kHz RTC Removal Mode

In low power mode a 32kHz clock is produced by a fractional-N divider (1st order Sigma Delta Modulated) to replace the traditional 32kHz XTAL. The capacitance is minimized for significant current reduced.

Parameter	Conditions	Min.	Nom.	Max.	Unit
Frequency	Averaged value		32768		Hz
XO LPM current consumption	Low power mode With all capacitors switched off and auto-amplitude calibration on		50		µA
Duty cycle				70	%
Settling time				5	ms
Frequency variation	After system calibration			±2	ppm
	Over temperature -30°C to 85°C			15	ppm
	Uncalibrated – total variation			200	ppm

3.2.14 Interrupt and Watchdog

3.2.14.1 Interrupt

Here are interrupt lists of PMIC to inform BB IC:

1. Key pressed and released interrupt
   - PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
   - FCHR_ENB: Interrupt is issued when FCHR_ENB is pressed (and released, set by the register). After receiving the interrupt, the software will read the FCHR_ENB _DEB status to see if it is pressed or released.
2. Thermal interrupt
   PMIC issues THR_H interrupt for the software high power latch if PMIC die temperature is over thermal regulation high threshold (e.g. 125°c) and issues THR_L for software latch release if PMIC die temperature goes from thermal regulation high threshold (e.g. 125°c) back to under thermal regulation low threshold (e.g. 110°c). The thermal regulation high/low threshold is adjustable.
3. Charger related interrupt
4. Battery voltage/current H/L interrupt
   There are two groups of VBAT detection interrupts.
   1) VBAT detected by AUXADC

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If VBAT is higher than the threshold specified by a register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.

2) VBAT detected by fuel gauge
If VBAT is higher than the threshold specified by a register setting, the VBAT_H interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the VBAT_L interrupt will be issued.

5. Fuel-Gauge
6. Buck OC interrupt
There are eight bucks and each has its individual interrupt which uses PWM detection method.
7. Buck PREOC interrupt
There are two buck preoc interrupts for VCORE and VGPU.
8. LDO OC interrupt
PMIC supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.
9. RTC interrupt
10. AUDIO interrupt
Audio interrupt can inform AP playback of the audio status.
11. ACCDET interrupt
This is for headphone detection.
12. HW JEITA interrupt
There are four HW JEITA interrupts for HOT/WARM/COOL/COLD threshold.
13. Novel Adaptive Fuel Gauge (NAFG) delta-V accumulation interrupt
If the accumulation of NAFG delta-voltage is larger than the programmable threshold, this interrupt will be issued.

3.2.15 Type-C

Type-C module supports USB Type-C connector. Measuring CC1/CC2 (newly added signal pins in Type-connector) voltage can determine:

a) Detect attach and detach event
b) Orientation
c) Power role
d) Source current ability

It has a close relationship with USB power Sourcing and Sinking, so the software driver must be combined with the USB power management part.
Type-C module is implemented based on CC state machine in Type-C SPEC V1.1. To support Source, Sink, DRP and Accessory mode, each type's state machine are combined (see Figure 3-13). Sink power sub-state machine (see Figure 3-14) is also implemented. Table 3-6 lists each type's supporting states. It is better to know the meaning of each state and what to do at each state before you start to use it.

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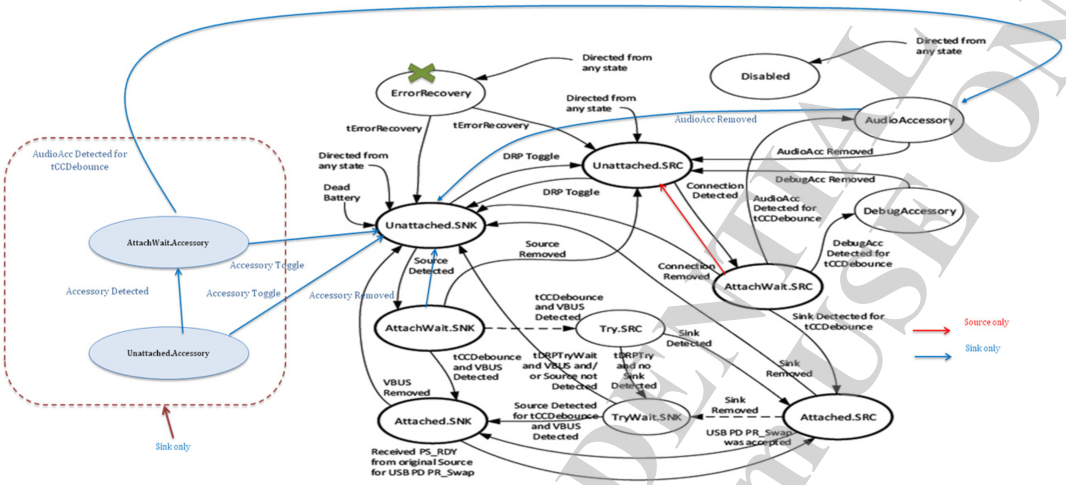

Figure 3-13. Type-C module target CC state machine

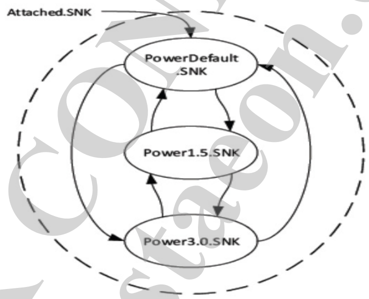

Figure 3-14. Type-C module target CC sub-power state

Table 3-6. Type-C module supported CC state

	SOURCE	SINK	DRP
Disabled	Support	Support	Support
Unattached.SNK	N/A	Support	Support
AttachWait.SNK	N/A	Support	Support
Attached.SNK	N/A	Support	Support
Unattached.SRC	Support	N/A	Support
AttachedWait.SRC	Support	N/A	Support
Attached.SRC	Support	N/A	Support
Try.SRC	N/A	N/A	Support
TryWait.SNK	N/A	N/A	Support
AudioAccessory	Support	Support	Support
DebugAccessory	Support	Support	Support
Unattached. Accessory	N/A	Support	N/A
AttachWait.Accessory	N/A	Support	N/A

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	SOURCE	SINK	DRP
PowerDefault.SNK	N/A	Support	Support
Power1.5.SNK	N/A	Support	Support
Power3.0.SNK	N/A	Support	Support

3.2.15.1 Watchdog Reset

WDTRSTB_IN is the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.2.16 SPI Interface

PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

On the other hand, the IO pin (MISO) can be used as data pin or interrupt pin depending on what the system scenario is. It is used as data pin when system is in normal mode but as INT pin when system is in suspend mode.

3.2.16.1 Data Format

The pre-defined SPI format consists of two modes: Single I/O mode and dual I/O mode. Single I/O always uses MOSI as output and input. Dual I/O uses both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction, 15-bit address (bit 15 to bit 1) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master is at the rising edge of the clock, and output data are at the falling edge of the clock. The parameter tSLCH, tDMMY and tCHSH are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

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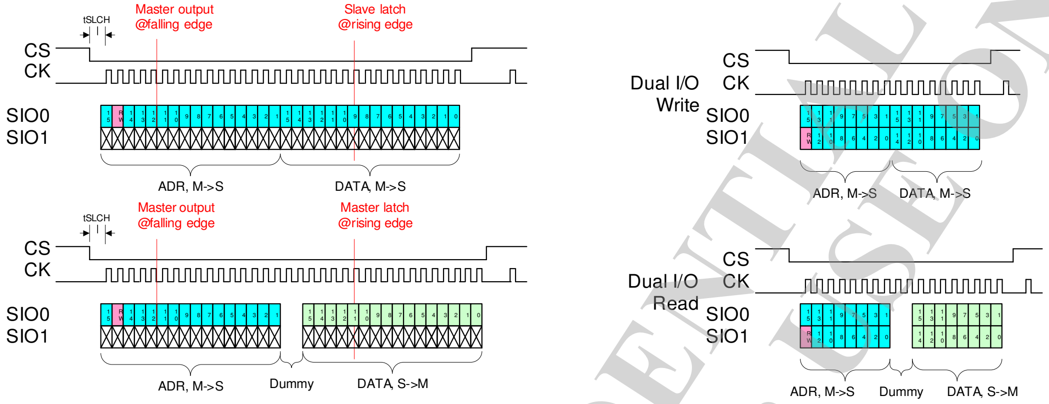
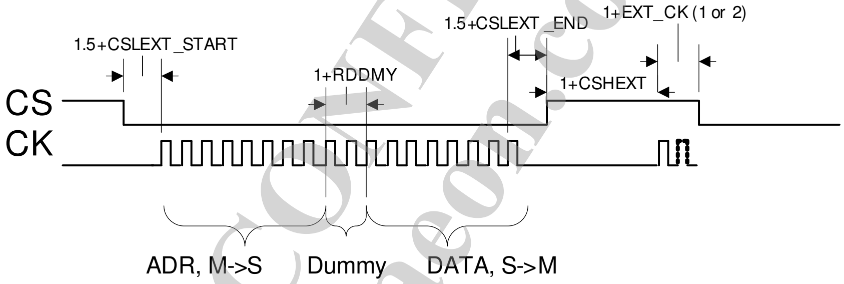
SPI format:



SPI parameter configuration:



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3.2.17 GPIO

3.2.17.1 GPIO List

Table 3-7. MT6353 GPIO list

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.5	Aux Func.6	Aux Func.7	PU/PD
PAD_SRCLKEN_IN0	GPIO0	**I1:SRCLKEN_IN0**			I0:TEST_IN0	O:TEST_OUT0	**PU**/PD
PAD_SRCLKEN_IN1	GPIO1	**I1:SRCLKEN_IN1**			I0:TEST_IN1	O:TEST_OUT1	**PU**/PD
PAD_RTC32K_1V8_0	GPIO2	**O:RTC_32K1V8_0**	O:INT_0	I0:TEST_CK0	I0:TEST_IN7	O:TEST_OUT7	PU/PD
PAD_RTC32K_1V8_1	GPIO3	**O:RTC_32K1V8_1**	O:INT_1	I0:TEST_CK2	I0:TEST_IN2	O:TEST_OUT2	PU/PD
PAD_SPI_CLK	GPIO4	**I0:SPI_CLK**					PU/**PD**
PAD_SPI_CSN	GPIO5	**I1:SPI_CSN**					**PU**/PD
PAD_SPI_MOSI	GPIO6	**B0:SPI_MOSI**					PU/PD
PAD_SPI_MISO	GPIO7	**B0:SPI_MISO**			I0:TEST_IN6	O:TEST_OUT6	PU/PD
PAD_AUD_CLK	GPIO8	**I0:AUD_CLK**		I0:TEST_CK1	I0:TEST_IN5	O:TEST_OUT5	PU/**PD**
PAD_AUD_DAT_MOSI	GPIO9	**I0:AUD_DAT_MOSI**			I0:TEST_IN3	O:TEST_OUT3	PU/**PD**
PAD_AUD_DAT_MISO	GPIO10	**O:AUD_DAT_MISO**			I0:TEST_IN4	O:TEST_OUT4	PU/**PD**

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3.2.17.2 GPIO Specification

Table 3-8. MT6353 GPIO electrical characteristics

Paramters	Descriptions	Min.	Typ.	Max.	Unit
Inputs					
VIH	Input logic low voltage	0.65*VDDQ		VDDQ+0.3	V
VIL	Input logic high voltage	-0.3		0.35*VDDQ	V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ
Outputs					
VOH(DC)	DC Output logic low voltage	0.75*VDDQ			V
VOL(DC)	DC Output logic high voltage			0.25*VDDQ	V
Leakage					
IIN	Input leakage current (any input 0V<VIN<VDDIO)	-5		5	mA
IOZ	Tri-state output leakage current	-5		5	mA
IIN	Input leakage current (VIN=3.3V/0V) for floating nwell IO	-10		10	mA
IOZ	Tri-state output leakage current for for floating nwell IO	-10		10	mA

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3.3 Register Table and Descriptions

Module name: PMIC_REG Base address: (+0h)

Address	Name	Width	Register Function
0000	STRUP_CON0	16	STRUP control register 0
0008	STRUP_CON4	16	STRUP control register 4
000A	STRUP_CON5	16	STRUP control register 5
000E	STRUP_CON7	16	STRUP control register 7
001A	STRUP_CON13	16	STRUP control register 13
0024	STRUP_ANA_CON0	16	STRUP_ANA_CON0
0026	STRUP_ANA_CON1	16	STRUP_ANA_CON1
0100	TYPE_C_PHY_RG_0	16	TYPE-C PHY RG 0
0102	TYPE_C_PHY_RG_CC_RESERVE_CSR	16	TYPE-C PHY RG CC Reserve CSR
0104	TYPE_C_VCMP_CTRL	16	TYPE-C Voltage Compare Control
0106	TYPE_C_CTRL	16	TYPE-C Control
010A	TYPE_C_CC_SW_CTRL	16	TYPE-C CC Stoftware Control
010C	TYPE_C_CC_VOL_PERIODIC_MEAS_VAL	16	TYPE-C CC Voltage Periodic Measure Value
010E	TYPE_C_CC_VOL_DEBOUCE_CNT_VAL	16	TYPE-C CC Voltage Debounce Count Value
0110	TYPE_C_DRP_SRC_CNT_VAL_0	16	TYPE-C DRP Source Count Value 0
0114	TYPE_C_DRP_SNK_CNT_VAL_0	16	TYPE-C DRP Sink Count Value 0
0118	TYPE_C_DRP_TRY_CNT_VAL_0	16	TYPE-C DRP Try Count Value 0
011C	TYPE_C_DRP_TRY_WAIT_CNT_VAL_0	16	TYPE-C DRP Try Wait Count Value 0
011E	TYPE_C_DRP_TRY_WAIT_CNT_VAL_1	16	TYPE-C DRP Try Wait Count Value 1
0120	TYPE_C_CC_SRC_DEFAULT_DAC_VAL	16	TYPE-C CC SRC Default DAC Value
0122	TYPE_C_CC_SRC_15_DAC_VAL	16	TYPE-C CC SRC 15 DAC Value
0124	TYPE_C_CC_SRC_30_DAC_VAL	16	TYPE-C CC SRC 30 DAC Value
0128	TYPE_C_CC_SNK_DAC_VAL	16	TYPE-C CC SNK DAC Value 0

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	0		
012A	TYPE_C_CC_SNK_DAC_VAL_1	16	TYPE-C CC SNK DAC Value 1
0130	TYPE_C_INTR_EN_0	16	TYPE-C Interrupt Enable 0
0134	TYPE_C_INTR_EN_2	16	TYPE-C Interrupt Enable 2
0138	TYPE_C_INTR_0	16	TYPE-C Interrupt 0
013C	TYPE_C_INTR_2	16	TYPE-C Interrupt 2
0140	TYPE_C_CC_STATUS	16	TYPE-C CC Status
0142	TYPE_C_PWR_STATUS	16	TYPE-C Power Status
0144	TYPE_C_PHY_RG_CC1_RESISTENCE_0	16	TYPE-C PHY RG CC1 Resistence_0
0146	TYPE_C_PHY_RG_CC1_RESISTENCE_1	16	TYPE-C PHY RG CC1 Resistence_1
0148	TYPE_C_PHY_RG_CC2_RESISTENCE_0	16	TYPE-C PHY RG CC2 Resistence_0
014A	TYPE_C_PHY_RG_CC2_RESISTENCE_1	16	TYPE-C PHY RG CC2 Resistence_1
0160	TYPE_C_CC_SW_FORCE_MODE_ENABLE	16	TYPE-C CC SW Force Mode Enable
0164	TYPE_C_CC_SW_FORCE_MODE_VAL_0	16	TYPE-C CC SW Force Mode Value_0
0166	TYPE_C_CC_SW_FORCE_MODE_VAL_1	16	TYPE-C CC SW Force Mode Value_1
0170	TYPE_C_CC_DAC_CALI_CTRL	16	TYPE-C CC DAC Calibration Control
0172	TYPE_C_CC_DAC_CALI_RESULT	16	TYPE-C CC DAC Calibration Result
0180	TYPE_C_DEBUG_PORT_SELECT_0	16	Debug Port Select 0
0182	TYPE_C_DEBUG_PORT_SELECT_1	16	Debug Port Select 1
0184	TYPE_C_DEBUG_MODE_SELECT	16	Debug Mode Select
0188	TYPE_C_DEBUG_OUT_READ_0	16	Debug Out Read 0
018A	TYPE_C_DEBUG_OUT_READ_1	16	Debug Out Read 1
0206	TEST_OUT	16	TEST_OUT

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020E	EN_STATUS1	16	Regulator status 1
0210	EN_STATUS2	16	Regulator status 2
021A	THERMALSTATUS	16	Thermal Status
021C	TOPSTATUS	16	TOP Status
021E	TDSEL_CON	16	TDSEL_CON
0220	RDSEL_CON	16	RDSEL_CON
0222	SMT_CON0	16	SMT_CON0
0224	SMT_CON1	16	SMT_CON1
0226	SMT_CON2	16	SMT_CON2
0228	DRV_CON0	16	DRV_CON0
022A	DRV_CON1	16	DRV_CON1
022C	DRV_CON2	16	DRV_CON2
022E	DRV_CON3	16	DRV_CON3
0230	TOP_STATUS	16	TOP_STATUS
0238	CLK_BUCK_CON0	16	CLK_BUCK control register 0
023A	CLK_BUCK_CON0_SET	16	CLK_BUCK control register 0_SET
023C	CLK_BUCK_CON0_CLR	16	CLK_BUCK control register 0_CLR
0240	CLK_BUCK_CON1_SET	16	CLK_BUCK control register 1_SET
0242	CLK_BUCK_CON1_CLR	16	CLK_BUCK control register 1_CLR
0244	TOP_CLKSQ	16	TOP_CLKSQ register
0246	TOP_CLKSQ_SET	16	TOP_CLKSQ register SET
0248	TOP_CLKSQ_CLR	16	TOP_CLKSQ register CLR
024A	TOP_CLKSQ_RTC	16	TOP_CLKSQ_RTC register
024C	TOP_CLKSQ_RTC_SET	16	TOP_CLKSQ_RTC register SET
024E	TOP_CLKSQ_RTC_CLR	16	TOP_CLKSQ_RTC register CLR
0250	TOP_CLK_TRIM	16	TOP_CLK_TRIM register
0256	CLK_PDN_CON0	16	CLK_PDN control register 0
0258	CLK_PDN_CON0_SET	16	CLK_PDN control register 0_SET
025A	CLK_PDN_CON0_CLR	16	CLK_PDN control register 0_CLR
025C	CLK_PDN_CON1	16	CLK_PDN control register 1
025E	CLK_PDN_CON1_SET	16	CLK_PDN control register 1_SET
0260	CLK_PDN_CON1_CLR	16	CLK_PDN control register 1_CLR
0262	CLK_SEL_CON0	16	CLK_SEL control register 0
0264	CLK_SEL_CON0_SET	16	CLK_SEL control register 0_SET

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0266	CLK_SEL_CON0_CLR	16	CLK_SEL control register 0_CLR
0268	CLK_SEL_CON1	16	CLK_SEL control register 1
026A	CLK_SEL_CON1_SET	16	CLK_SEL control register 1_SET
026C	CLK_SEL_CON1_CLR	16	CLK_SEL control register 1_CLR
026E	CLK_CKPDN_CON0	16	CLK_CKPDN control register 0
0270	CLK_CKPDN_CON0_SET	16	CLK_CKPDN SET control register 0
0272	CLK_CKPDN_CON0_CLR	16	CLK_CKPDN CLR control register 0
0274	CLK_CKPDN_CON1	16	CLK_CKPDN control register 1
0276	CLK_CKPDN_CON1_SET	16	CLK_CKPDN SET control register 1
0278	CLK_CKPDN_CON1_CLR	16	CLK_CKPDN CLR control register 1
027A	CLK_CKPDN_CON2	16	CLK_CKPDN control register 2
027C	CLK_CKPDN_CON2_SET	16	CLK_CKPDN SET control register 2
027E	CLK_CKPDN_CON2_CLR	16	CLK_CKPDN CLR control register 2
0280	CLK_CKPDN_CON3	16	CLK_CKPDN control register 3
0282	CLK_CKPDN_CON3_SET	16	CLK_CKPDN SET control register 3
0284	CLK_CKPDN_CON3_CLR	16	CLK_CKPDN CLR control register 3
0286	CLK_CKPDN_HWEN_CON0	16	CLK_CKPDN_HWEN control register 0
0288	CLK_CKPDN_HWEN_CON0_SET	16	CLK_CKPDN_HWEN SET control register 0
028A	CLK_CKPDN_HWEN_CON0_CLR	16	CLK_CKPDN_HWEN CLR control register 0
028C	CLK_CKSEL_CON0	16	CLK_CKSEL control register 0
028E	CLK_CKSEL_CON0_SET	16	CLK_CKSEL SET control register 0
0290	CLK_CKSEL_CON0_CLR	16	CLK_CKSEL CLR control register 0
0292	CLK_CKDIVSEL_CON0	16	CLK_CKDIVSEL control register 0
0294	CLK_CKDIVSEL_CON0_SET	16	CLK_CKDIVSEL SET control register 0
0296	CLK_CKDIVSEL_CON0_CLR	16	CLK_CKDIVSEL CLR control register 0
02AE	TOP_RST_STATUS	16	TOP_RST_STATUS register
02E0	SPK_CON0	16	Speaker Control Register 0
02E2	SPK_CON1	16	Speaker Control Register 1
02E4	SPK_CON2	16	Speaker Control Register 2

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02EC	SPK_CON6	16	Speaker Control Register 6
02EE	SPK_CON7	16	Speaker Control Register 7
02F0	SPK_CON8	16	Speaker Control Register 8
02F2	SPK_CON9	16	Speaker Control Register 9
02F4	SPK_CON10	16	Speaker Control Register 10
02F6	SPK_CON11	16	Speaker Control Register 11
02F8	SPK_CON12	16	Speaker Control Register 12
02FA	SPK_CON13	16	Speaker Control Register 13
02FC	SPK_CON14	16	Speaker Control Register 14
02FE	SPK_CON15	16	Speaker Control Register 15
0300	SPK_CON16	16	Speaker Control Register 16
0302	SPK_ANA_CON0	16	SPK Control Register 0
0304	SPK_ANA_CON1	16	SPK Control Register 1
0306	SPK_ANA_CON3	16	SPK Control Register 3
0310	ISINK0_CON0	16	ISINK0 Control Register 0
0312	ISINK0_CON1	16	ISINK0 Control Register 1
0314	ISINK0_CON2	16	ISINK0 Control Register 2
0316	ISINK0_CON3	16	ISINK0 Control Register 3
0318	ISINK1_CON0	16	ISINK1 Control Register 0
031A	ISINK1_CON1	16	ISINK1 Control Register 1
031C	ISINK1_CON2	16	ISINK1 Control Register 2
031E	ISINK1_CON3	16	ISINK1 Control Register 3
0324	ISINK_SFSTR	16	ISINK SOFT START
0326	ISINK_EN_CTRL	16	ISINK Enable control
0328	ISINK_MODE_CTRL	16	ISINK mode control
032A	ISINK_ANA_CON0	16	ISINK control register 0
0334	CHRIND_CON0	16	CHRIND Control Register 0
0336	CHRIND_CON1	16	CHRIND Control Register 1
0338	CHRIND_CON2	16	CHRIND Control Register 2
033A	CHRIND_CON3	16	CHRIND Control Register 3
033C	CHRIND_EN_CTRL	16	CHRIND Enable control simple
041E	BUCK_OC_CON0	16	BUCK_OC control register 0
0424	BUCK_OC_CON3	16	BUCK_OC control register 3
0426	BUCK_OC_CON4	16	BUCK_OC control register 4
0432	SMPS_TOP_ANA_CON0	16	SMPS_TOP control register 0
0434	SMPS_TOP_ANA_CON1	16	SMPS_TOP control register 1
0436	SMPS_TOP_ANA_CON2	16	SMPS_TOP control register 2
0438	SMPS_TOP_ANA_CON3	16	SMPS_TOP control register 3

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043A	SMPS_TOP_ANA_CON4	16	SMPS_TOP control register 4
043C	SMPS_TOP_ANA_CON5	16	SMPS_TOP control register 5
043E	SMPS_TOP_ANA_CON6	16	SMPS_TOP control register 6
0440	VPA_ANA_CON0	16	VPA control register 0
0442	VPA_ANA_CON1	16	VPA control register 1
0444	VPA_ANA_CON2	16	VPA control register 2
0446	VPA_ANA_CON3	16	VPA control register 3
0448	VCORE_ANA_CON0	16	VCORE control register 0
044A	VCORE_ANA_CON1	16	VCORE control register 1
044C	VCORE_ANA_CON2	16	VCORE control register 2
044E	VCORE_ANA_CON3	16	VCORE control register 3
0450	VCORE_ANA_CON4	16	VCORE control register 4
0452	VPROC_ANA_CON0	16	VPROC control register 0
0454	VPROC_ANA_CON1	16	VPROC control register 1
0456	VPROC_ANA_CON2	16	VPROC control register 2
0458	VPROC_ANA_CON3	16	VPROC control register 3
045A	VPROC_ANA_CON4	16	VPROC control register 4
045C	VS1_ANA_CON0	16	VS1 control register 0
045E	VS1_ANA_CON1	16	VS1 control register 1
0460	VS1_ANA_CON2	16	VS1 control register 2
0462	VS1_ANA_CON3	16	VS1 control register 3
0464	VS1_ANA_CON4	16	VS1 control register 4
0466	BUCK_ANA_CON0	16	BUCK_ANA_CON0
0468	BUCK_ANA_CON1	16	BUCK_ANA_CON1
046A	VCORE2_ANA_CON0	16	VCORE2 control register 0
046C	VCORE2_ANA_CON1	16	VCORE2 control register 1
046E	VCORE2_ANA_CON2	16	VCORE2 control register 2
0470	VCORE2_ANA_CON3	16	VCORE2 control register 3
0472	VCORE2_ANA_	16	VCORE2 control register 4

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	CON4		
0604	BUCK_VPROC_EN_CON0	16	BUCK VPROC ENABLE CON0
0608	BUCK_VPROC_VOL_CON0	16	BUCK VPROC VOLTAGE CON0
060A	BUCK_VPROC_VOL_CON1	16	BUCK VPROC VOLTAGE CON1
060C	BUCK_VPROC_VOL_CON2	16	BUCK VPROC VOLTAGE CON2
0612	BUCK_VS1_HWM_CON0	16	BUCK VS1 HW MODE CON0
0614	BUCK_VS1_HWM_CON0_SET	16	BUCK_VS1_HWM control register 0_SET
0616	BUCK_VS1_HWM_CON0_CLR	16	BUCK_VS1_HWM control register 0_CLR
061A	BUCK_VS1_EN_CON0	16	BUCK VS1 ENABLE CON0
061E	BUCK_VS1_VOL_CON0	16	BUCK VS1 VOLTAGE CON0
0620	BUCK_VS1_VOL_CON1	16	BUCK VS1 VOLTAGE CON1
0622	BUCK_VS1_VOL_CON2	16	BUCK VS1 VOLTAGE CON2
062C	BUCK_VCORE_EN_CON0	16	BUCK VCORE ENABLE CON0
0630	BUCK_VCORE_VOL_CON0	16	BUCK VCORE VOLTAGE CON0
0632	BUCK_VCORE_VOL_CON1	16	BUCK VCORE VOLTAGE CON1
0634	BUCK_VCORE_VOL_CON2	16	BUCK VCORE VOLTAGE CON2
063E	BUCK_VCORE2_EN_CON0	16	BUCK VCORE2 ENABLE CON0
0642	BUCK_VCORE2_VOL_CON0	16	BUCK VCORE2 VOLTAGE CON0
0644	BUCK_VCORE2_VOL_CON1	16	BUCK VCORE2 VOLTAGE CON1
0646	BUCK_VCORE2_VOL_CON2	16	BUCK VCORE2 VOLTAGE CON2
064C	BUCK_VPA_EN_CON0	16	BUCK VPA ENABLE CON0
0650	BUCK_VPA_VOL_CON0	16	BUCK VPA VOLTAGE CON0
0652	BUCK_VPA_VOL_CON1	16	BUCK VPA VOLTAGE CON1
0800	ZCD_CON0	16	ZCD control register 0
0802	ZCD_CON1	16	ZCD control register 1
0804	ZCD_CON2	16	ZCD control register 2
0806	ZCD_CON3	16	ZCD control register 3
0808	ZCD_CON4	16	ZCD control register 4
080A	ZCD_CON5	16	ZCD control register 5
0A04	LDO_TOP_CON0	16	LDO VA18 control register 1
0A0C	VRTC_CON0	16	VRTC control register 0

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0A0E	LDO_SHARE_VCN33_CON0	16	LDO_SHARE_VCN33_CON0
0A10	LDO_SHARE_VCN33_CON1	16	LDO_SHARE_VCN33_CON1
0A12	LDO3_VCN33_CON0	16	LDO VCN33 control register 0
0A14	LDO3_VCN33_OCFB_CON0	16	LDO VCN33 control register 1
0A1A	LDO1_VLDO28_CON0	16	LDO VLDO28 control register 0
0A1C	LDO1_VLDO28_OCFB_CON0	16	LDO VLDO28 control register 1
0A24	LDO_VSRAM_PROC_VOL_CON0	16	LDO VSRAM_PROC VOLTAGE CON0
0A26	LDO_VSRAM_PROC_VOL_CON1	16	LDO VSRAM_PROC VOLTAGE CON1
0A28	LDO_VSRAM_PROC_VOL_CON2	16	LDO VSRAM_PROC VOLTAGE CON2
0A2E	LDO_BATON_CON0	16	LDO_BATON_CON0
0A30	LDO2_TREF_CON0	16	LDO TREF control register 0
0A32	LDO3_VTCXO28_CON0	16	LDO VTCXO28 control register 0
0A34	LDO3_VTCXO28_OCFB_CON0	16	LDO VTCXO28 control register 1
0A36	LDO3_VTCXO24_CON0	16	LDO VTCXO24 control register 0
0A38	LDO3_VTCXO24_OCFB_CON0	16	LDO VTCXO24 control register 1
0A3A	LDO3_VXO22_CON0	16	LDO VXO22 control register 0
0A3C	LDO3_VXO22_OCFB_CON0	16	LDO VXO22 control register 1
0A3E	LDO3_VRF18_CON0	16	LDO VRF18 control register 0
0A40	LDO3_VRF18_OCFB_CON0	16	LDO VRF18 control register 1
0A42	LDO3_VRF12_CON0	16	LDO VRF12 control register 0
0A44	LDO3_VRF12_OCFB_CON0	16	LDO VRF12 control register 1
0A48	LDO3_VCN28_CON0	16	LDO VCN28 control register 0
0A4A	LDO3_VCN28_OCFB_CON0	16	LDO VCN28 control register 1
0A4C	LDO3_VCN18_CON0	16	LDO VCN18 control register 0
0A4E	LDO3_VCN18_OCFB_CON0	16	LDO VCN18 control register 1
0A50	LDO0_VCAMA_CON0	16	LDO VCAMA control register 0
0A52	LDO0_VCAMA_OCFB_CON0	16	LDO VCAMA control register 1

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0A54	LDO0_VCAMIO_CON0	16	LDO VCAMIO control register 0
0A56	LDO0_VCAMIO_OCFB_CON0	16	LDO VCAMIO control register 1
0A58	LDO0_VCAMD_CON0	16	LDO VCAMD control register 0
0A5A	LDO0_VCAMD_OCFB_CON0	16	LDO VCAMD control register 1
0A5C	LDO3_VAUX18_CON0	16	LDO VAUX18 control register 0
0A5E	LDO3_VAUX18_OCFB_CON0	16	LDO VAUX18 control register 1
0A60	LDO3_VAUD28_CON0	16	LDO VAUD28 control register 0
0A62	LDO3_VAUD28_OCFB_CON0	16	LDO VAUD28 control register 1
0A64	LDO3_VSRAM_PROC_CON0	16	LDO VSRAM_PROC control register 0
0A66	LDO3_VSRAM_PROC_OCFB_CON0	16	LDO VSRAM_PROC control register 1
0A68	LDO1_VDRAM_CON0	16	LDO VDRAM control register 0
0A6A	LDO1_VDRAM_OCFB_CON0	16	LDO VDRAM control register 1
0A6E	LDO1_VSIM1_CON0	16	LDO VSIM1 control register 0
0A70	LDO1_VSIM1_OCFB_CON0	16	LDO VSIM1 control register 1
0A72	LDO1_VSIM2_CON0	16	LDO VSIM2 control register 0
0A74	LDO1_VSIM2_OCFB_CON0	16	LDO VSIM2 control register 1
0A76	LDO1_VIO28_CON0	16	LDO VIO28 control register 0
0A78	LDO1_VIO28_OCFB_CON0	16	LDO VIO28 control register 1
0A7A	LDO1_VMC_CON0	16	LDO VMC control register 0
0A7C	LDO1_VMC_OCFB_CON0	16	LDO VMC control register 1
0A80	LDO1_VMCH_CON0	16	LDO VMCH control register 0
0A82	LDO1_VMCH_OCFB_CON0	16	LDO VMCH control register 1
0A86	LDO1_VUSB33_CON0	16	LDO VUSB33 control register 0
0A88	LDO1_VUSB33_OCFB_CON0	16	LDO VUSB33 control register 1
0A8A	LDO1_VEMC33_CON0	16	LDO VEMC33 control register 0
0A8C	LDO1_VEMC33_OCFB_CON0	16	LDO VEMC33 control register 1
0A90	LDO1_VIO18_CON0	16	LDO VIO18 control register 0
0A92	LDO1_VIO18_OCFB_CON0	16	LDO VIO18 control register 1

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0A94	LDO0_VIBR_CON0	16	LDO VIBR control register 0
0A96	LDO0_VIBR_OCFB_CON0	16	LDO VIBR control register 1
0A98	ALDO_ANA_CON0	16	ALDO control register 0
0A9A	ALDO_ANA_CON1	16	ALDO control register 1
0A9C	ALDO_ANA_CON2	16	ALDO control register 2
0A9E	ALDO_ANA_CON3	16	ALDO control register 3
0AA0	ALDO_ANA_CON4	16	ALDO control register 4
0AA2	ALDO_ANA_CON5	16	ALDO control register 5
0AA4	ALDO_ANA_CON6	16	ALDO control register 6
0AA6	DLDO_ANA_CON0	16	DLDO control register 0
0AA8	DLDO_ANA_CON1	16	DLDO control register 1
0AAA	DLDO_ANA_CON2	16	DLDO control register 2
0AAC	DLDO_ANA_CON3	16	DLDO control register 3
0AAE	DLDO_ANA_CON4	16	DLDO control register 4
0AB0	DLDO_ANA_CON5	16	DLDO control register 5
0AB2	DLDO_ANA_CON6	16	DLDO control register 6
0AB4	DLDO_ANA_CON7	16	DLDO control register 7
0AB6	DLDO_ANA_CON8	16	DLDO control register 8
0AB8	DLDO_ANA_CON9	16	DLDO control register 9
0ABA	DLDO_ANA_CON10	16	DLDO control register 10
0ABC	DLDO_ANA_CON11	16	DLDO control register 11
0ABE	DLDO_ANA_CON12	16	DLDO control register 12
0AC0	DLDO_ANA_CON13	16	DLDO control register 13
0AC2	DLDO_ANA_CON14	16	DLDO control register 14
0AC4	DLDO_ANA_CON15	16	DLDO control register 15
0AC6	DLDO_ANA_CON16	16	DLDO control register 16
0AC8	DLDO_ANA_CON17	16	DLDO control register 17
0ACA	SLDO_ANA_CON0	16	SLDO control register 0
0ACC	SLDO_ANA_CO	16	SLDO control register 1

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	N1		
0ACE	SLDO_ANA_CON2	16	SLDO control register 2
0AD0	SLDO_ANA_CON3	16	SLDO control register 3
0AD2	SLDO_ANA_CON4	16	SLDO control register 4
0AD4	SLDO_ANA_CON5	16	SLDO control register 5
0AD6	SLDO_ANA_CON6	16	SLDO control register 6
0AD8	SLDO_ANA_CON7	16	SLDO control register 7
0ADA	SLDO_ANA_CON8	16	SLDO control register 8
0ADC	SLDO_ANA_CON9	16	SLDO control register 9
0ADE	SLDO_ANA_CON10	16	SLDO control register 10
0C00	OTP_CON0	16	OTP control register 0
0C02	OTP_CON1	16	OTP control register 1
0C04	OTP_CON2	16	OTP control register 2
0C06	OTP_CON3	16	OTP control register 3
0C08	OTP_CON4	16	OTP control register 4
0C0A	OTP_CON5	16	OTP control register 5
0C0C	OTP_CON6	16	OTP control register 6
0C0E	OTP_CON7	16	OTP control register 7
0C10	OTP_CON8	16	OTP control register 8
0C12	OTP_CON9	16	OTP control register 9
0C14	OTP_CON10	16	OTP control register 10
0C16	OTP_CON11	16	OTP control register 11
0C18	OTP_CON12	16	OTP control register 12
0C1A	OTP_CON13	16	OTP control register 13
0C1C	OTP_CON14	16	OTP control register 14
0C1E	OTP_DOUT_0_15	16	OTP dout 0 15
0C20	OTP_DOUT_16_31	16	OTP dout 16 31
0C22	OTP_DOUT_32_47	16	OTP dout 32 47
0C24	OTP_DOUT_48_63	16	OTP dout 48 63
0C26	OTP_DOUT_64_79	16	OTP dout 64 79
0C28	OTP_DOUT_80_95	16	OTP dout 80 95
0C2A	OTP_DOUT_96_111	16	OTP dout 96 111
0C2C	OTP_DOUT_112_127	16	OTP dout 112 127
0C2E	OTP_DOUT_128_143	16	OTP dout 128 143
0C30	OTP_DOUT_144_159	16	OTP dout 144 159

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0C32	OTP_DOUT_160_175	16	OTP dout 160 175
0C34	OTP_DOUT_176_191	16	OTP dout 176 191
0C36	OTP_DOUT_192_207	16	OTP dout 192 207
0C38	OTP_DOUT_208_223	16	OTP dout 208 223
0C3A	OTP_DOUT_224_239	16	OTP dout 224 239
0C3C	OTP_DOUT_240_255	16	OTP dout 240 255
0C3E	OTP_DOUT_256_271	16	OTP dout 256 271
0C40	OTP_DOUT_272_287	16	OTP dout 272 287
0C42	OTP_DOUT_288_303	16	OTP dout 288 303
0C44	OTP_DOUT_304_319	16	OTP dout 304 319
0C46	OTP_DOUT_320_335	16	OTP dout 320 335
0C48	OTP_DOUT_336_351	16	OTP dout 336 351
0C4A	OTP_DOUT_352_367	16	OTP dout 352 367
0C4C	OTP_DOUT_368_383	16	OTP dout 368 383
0C4E	OTP_DOUT_384_399	16	OTP dout 384 399
0C50	OTP_DOUT_400_415	16	OTP dout 400 415
0C52	OTP_DOUT_416_431	16	OTP dout 416 431
0C54	OTP_DOUT_432_447	16	OTP dout 432 447
0C56	OTP_DOUT_448_463	16	OTP dout 448 463
0C58	OTP_DOUT_464_479	16	OTP dout 464 479
0C5A	OTP_DOUT_480_495	16	OTP dout 480 495
0C5C	OTP_DOUT_496_511	16	OTP dout 496 511
0C5E	OTP_VAL_0_15	16	OTP val 0 15
0C60	OTP_VAL_16_31	16	OTP val 16 31
0C62	OTP_VAL_32_47	16	OTP val 32 47
0C64	OTP_VAL_48_63	16	OTP val 48 63
0C66	OTP_VAL_64_79	16	OTP val 64 79
0C68	OTP_VAL_80_95	16	OTP val 80 95
0C6A	OTP_VAL_96_111	16	OTP val 96 111

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0C6C	OTP_VAL_112_127	16	OTP val 112 127
0C6E	OTP_VAL_128_143	16	OTP val 128 143
0C70	OTP_VAL_144_159	16	OTP val 144 159
0C72	OTP_VAL_160_175	16	OTP val 160 175
0C74	OTP_VAL_176_191	16	OTP val 176 191
0C76	OTP_VAL_192_207	16	OTP val 192 207
0C78	OTP_VAL_208_223	16	OTP val 208 223
0C7A	OTP_VAL_224_239	16	OTP val 224 239
0C7C	OTP_VAL_240_255	16	OTP val 240 255
0C7E	OTP_VAL_256_271	16	OTP val 256 271
0C80	OTP_VAL_272_287	16	OTP val 272 287
0C82	OTP_VAL_288_303	16	OTP val 288 303
0C84	OTP_VAL_304_319	16	OTP val 304 319
0C86	OTP_VAL_320_335	16	OTP val 320 335
0C88	OTP_VAL_336_351	16	OTP val 336 351
0C8A	OTP_VAL_352_367	16	OTP val 352 367
0C8C	OTP_VAL_368_383	16	OTP val 368 383
0C8E	OTP_VAL_384_399	16	OTP val 384 399
0C90	OTP_VAL_400_415	16	OTP val 400 415
0C92	OTP_VAL_416_431	16	OTP val 416 431
0C94	OTP_VAL_432_447	16	OTP val 432 447
0C96	OTP_VAL_448_463	16	OTP val 448 463
0C98	OTP_VAL_464_479	16	OTP val 464 479
0C9A	OTP_VAL_480_495	16	OTP val 480 495
0C9C	OTP_VAL_496_511	16	OTP val 496 511
0CA6	FGADC_CON1	16	FGADC control register 1
0CA8	FGADC_CON2	16	FGADC control register 2
0CAA	FGADC_CON3	16	FGADC control register 3
0CAC	FGADC_CON4	16	FGADC control register 4
0CAE	FGADC_CON5	16	FGADC control register 5
0CB0	FGADC_CON6	16	FGADC control register 6

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0CBA	FGADC_CON11	16	FGADC control register 11
0CC0	FGADC_CON14	16	FGADC control register 14
0CF2	AUDDEC_ANA_CON0	16	AUDDEC control register 0
0CF4	AUDDEC_ANA_CON1	16	AUDDEC control register 1
0CF6	AUDDEC_ANA_CON2	16	AUDDEC control register 2
0CF8	AUDDEC_ANA_CON3	16	AUDDEC control register 3
0CFA	AUDDEC_ANA_CON4	16	AUDDEC control register 4
0CFC	AUDDEC_ANA_CON5	16	AUDDEC control register 5
0CFE	AUDDEC_ANA_CON6	16	AUDDEC control register 6
0D00	AUDDEC_ANA_CON7	16	AUDDEC control register 7
0D02	AUDDEC_ANA_CON8	16	AUDDEC control register 8
0D04	AUDENC_ANA_CON0	16	AUDENC control register 0
0D06	AUDENC_ANA_CON1	16	AUDENC control register 1
0D08	AUDENC_ANA_CON2	16	AUDENC control register 2
0D0A	AUDENC_ANA_CON3	16	AUDENC control register 3
0D0C	AUDENC_ANA_CON4	16	AUDENC control register 4
0D0E	AUDENC_ANA_CON5	16	AUDENC control register 5
0D10	AUDENC_ANA_CON6	16	AUDENC control register 6
0D12	AUDENC_ANA_CON7	16	AUDENC control register 7
0D14	AUDENC_ANA_CON8	16	AUDENC control register 8
0D16	AUDENC_ANA_CON9	16	AUDENC control register 9
0D18	AUDENC_ANA_CON10	16	AUDENC control register 10
0D1A	AUDNCP_CLKDIV_CON0	16	AUDNCP_CLKDIV control register 0
0D1C	AUDNCP_CLKDIV_CON1	16	AUDNCP_CLKDIV control register 1
0D1E	AUDNCP_CLKDIV_CON2	16	AUDNCP_CLKDIV control register 2
0D20	AUDNCP_CLKDIV_CON3	16	AUDNCP_CLKDIV control register 3
0D22	AUDNCP_CLKDIV_CON4	16	AUDNCP_CLKDIV control register 4
0D24	DCXO_CW00	16	DCXO Code Word 0
0D26	DCXO_CW00_SET	16	DCXO Code Word 0 Set
0D28	DCXO_CW00_	16	DCXO Code Word 0 Clear

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	CLR		
0D2A	DCXO_CW01	16	DCXO Code Word 1
0D2C	DCXO_CW02	16	DCXO Code Word 2
0D2E	DCXO_CW03	16	DCXO Code Word 3
0D30	DCXO_CW04	16	DCXO Code Word 4
0D32	DCXO_CW05	16	DCXO Code Word 5
0D34	DCXO_CW06	16	DCXO Code Word 6
0D36	DCXO_CW07	16	DCXO Code Word 7
0D38	DCXO_CW08	16	DCXO Code Word 8
0D3A	DCXO_CW09	16	DCXO Code Word 9
0D3C	DCXO_CW10	16	DCXO Code Word 10
0D3E	DCXO_CW11	16	DCXO Code Word 11
0D40	DCXO_CW12	16	DCXO Code Word 12
0D42	DCXO_CW13	16	DCXO Code Word 13
0D44	DCXO_CW14	16	DCXO Code Word 14
0D46	DCXO_CW15	16	DCXO Code Word 15
0D48	DCXO_CW16	16	DCXO Code Word 16
0E00	AUXADC_ADC0	16	AUXADC ADC register 0
0E02	AUXADC_ADC1	16	AUXADC ADC register 1
0E04	AUXADC_ADC2	16	AUXADC ADC register 2
0E06	AUXADC_ADC3	16	AUXADC ADC register 3
0E08	AUXADC_ADC4	16	AUXADC ADC register 4
0E0A	AUXADC_ADC5	16	AUXADC ADC register 5
0E0C	AUXADC_ADC6	16	AUXADC ADC register 6
0E0E	AUXADC_ADC7	16	AUXADC ADC register 7
0E10	AUXADC_ADC8	16	AUXADC ADC register 8
0E12	AUXADC_ADC9	16	AUXADC ADC register 9
0E14	AUXADC_ADC10	16	AUXADC ADC register 10
0E16	AUXADC_ADC11	16	AUXADC ADC register 11
0E18	AUXADC_ADC12	16	AUXADC ADC register 12
0E1A	AUXADC_ADC13	16	AUXADC ADC register 13
0E1C	AUXADC_ADC14	16	AUXADC ADC register 14
0E1E	AUXADC_ADC15	16	AUXADC ADC register 15
0E20	AUXADC_ADC16	16	AUXADC ADC register 16
0E22	AUXADC_ADC17	16	AUXADC ADC register 17
0E24	AUXADC_ADC18	16	AUXADC ADC register 18
0E26	AUXADC_ADC19	16	AUXADC ADC register 19

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0E28	AUXADC_ADC20	16	AUXADC ADC register 20
0E2A	AUXADC_ADC21	16	AUXADC ADC register 21
0E2C	AUXADC_ADC22	16	AUXADC ADC register 22
0E2E	AUXADC_ADC23	16	AUXADC ADC register 23
0E30	AUXADC_ADC24	16	AUXADC ADC register 24
0E32	AUXADC_ADC25	16	AUXADC ADC register 25
0E34	AUXADC_ADC26	16	AUXADC ADC register 26
0E36	AUXADC_ADC27	16	AUXADC ADC register 27
0E38	AUXADC_ADC28	16	AUXADC ADC register 28
0E3A	AUXADC_ADC29	16	AUXADC ADC register 29
0E3C	AUXADC_ADC30	16	AUXADC ADC register 30
0E3E	AUXADC_ADC31	16	AUXADC ADC register 31
0E40	AUXADC_ADC32	16	AUXADC ADC register 32
0E42	AUXADC_ADC33	16	AUXADC ADC register 33
0E44	AUXADC_ADC34	16	AUXADC ADC register 34
0E46	AUXADC_ADC35	16	AUXADC ADC register 35
0E48	AUXADC_ADC36	16	AUXADC ADC register 36
0E4A	AUXADC_ADC37	16	AUXADC ADC register 37
0E4C	AUXADC_ADC38	16	AUXADC ADC register 38
0E4E	AUXADC_ADC39	16	AUXADC ADC register 39
0E50	AUXADC_ADC40	16	AUXADC ADC register 40
0E52	AUXADC_BUF0	16	AUXADC_BUF0
0E54	AUXADC_BUF1	16	AUXADC_BUF1
0E56	AUXADC_BUF2	16	AUXADC_BUF2
0E58	AUXADC_BUF3	16	AUXADC_BUF3
0E5A	AUXADC_BUF4	16	AUXADC_BUF4
0E5C	AUXADC_BUF5	16	AUXADC_BUF5
0E5E	AUXADC_BUF6	16	AUXADC_BUF6
0E60	AUXADC_BUF7	16	AUXADC_BUF7
0E62	AUXADC_BUF8	16	AUXADC_BUF8
0E64	AUXADC_BUF9	16	AUXADC_BUF9
0E66	AUXADC_BUF10	16	AUXADC_BUF10

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0E68	AUXADC_BUF11	16	AUXADC_BUF11
0E6A	AUXADC_BUF12	16	AUXADC_BUF12
0E6C	AUXADC_BUF13	16	AUXADC_BUF13
0E6E	AUXADC_BUF14	16	AUXADC_BUF14
0E70	AUXADC_BUF15	16	AUXADC_BUF15
0E72	AUXADC_BUF16	16	AUXADC_BUF16
0E74	AUXADC_BUF17	16	AUXADC_BUF17
0E76	AUXADC_BUF18	16	AUXADC_BUF18
0E78	AUXADC_BUF19	16	AUXADC_BUF19
0E7A	AUXADC_BUF20	16	AUXADC_BUF20
0E7C	AUXADC_BUF21	16	AUXADC_BUF21
0E7E	AUXADC_BUF22	16	AUXADC_BUF22
0E80	AUXADC_BUF23	16	AUXADC_BUF23
0E82	AUXADC_BUF24	16	AUXADC_BUF24
0E84	AUXADC_BUF25	16	AUXADC_BUF25
0E86	AUXADC_BUF26	16	AUXADC_BUF26
0E88	AUXADC_BUF27	16	AUXADC_BUF27
0E8A	AUXADC_BUF28	16	AUXADC_BUF28
0E8C	AUXADC_BUF29	16	AUXADC_BUF29
0E8E	AUXADC_BUF30	16	AUXADC_BUF30
0E90	AUXADC_BUF31	16	AUXADC_BUF31
0E92	AUXADC_STA0	16	AUXADC_STA0
0E94	AUXADC_STA1	16	AUXADC_STA1
0E96	AUXADC_STA2	16	AUXADC_STA2
0EC0	AUXADC_CON12	16	AUXADC_CON12
0F58	ACCDET_CON0	16	ACCDET control register 0
0F5A	ACCDET_CON1	16	ACCDET control register 1
0F5C	ACCDET_CON2	16	ACCDET control register 2
0F5E	ACCDET_CON3	16	ACCDET control register 3
0F60	ACCDET_CON4	16	ACCDET control register 4
0F62	ACCDET_CON5	16	ACCDET control register 5
0F64	ACCDET_CON6	16	ACCDET control register 6
0F66	ACCDET_CON7	16	ACCDET control register 7

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0F68	ACCDET_CON8	16	ACCDET control register 8
0F6A	ACCDET_CON9	16	ACCDET control register 9
0F6C	ACCDET_CON10	16	ACCDET control register 10
0F70	ACCDET_CON12	16	ACCDET control register 12
0F74	ACCDET_CON14	16	ACCDET control register 14
0F76	ACCDET_CON15	16	ACCDET control register 15
0F78	ACCDET_CON16	16	ACCDET control register 16
0F7E	ACCDET_CON19	16	ACCDET control register 19
0F8C	CHR_CON0	16	Charger control register 0
0F8E	CHR_CON1	16	Charger Control Register 1
0F90	CHR_CON2	16	Charger Control Register 2
0F92	CHR_CON3	16	Charger Control Register 3
0F94	CHR_CON4	16	Charger Control Register 4
0F98	CHR_CON6	16	Charger Control Register 6
0F9A	CHR_CON7	16	Charger Control Register 7
0F9E	CHR_CON9	16	Charger Control Register 9
0FA0	CHR_CON10	16	Charger Control Register 10
0FA6	CHR_CON13	16	Charger Control Register 13
0FAA	CHR_CON15	16	Charger Control Register 15
0FAC	CHR_CON16	16	Charger Control Register 16
0FAE	CHR_CON17	16	Charger Control Register 17
0FB0	CHR_CON18	16	Charger Control Register 18
0FB2	CHR_CON19	16	Charger Control Register 19
0FB4	CHR_CON20	16	Charger Control Register 20
0FB6	CHR_CON21	16	Charger Control Register 21
0FBA	CHR_CON23	16	Charger Control Register 23
0FBC	CHR_CON24	16	Charger Control Register 24
0FBE	CHR_CON25	16	Charger Control Register 25
0FC8	CHR_CON30	16	Charger Control Register 30
0FCA	CHR_CON31	16	Charger Control Register 31
0FCC	CHR_CON32	16	Charger Control Register 32
0FCE	CHR_CON33	16	Charger Control Register 33
0FD0	CHR_CON34	16	Charger Control Register 34
0FD2	CHR_CON35	16	Charger Control Register 35
0FD4	CHR_CON36	16	Charger Control Register 36
0FD6	CHR_CON37	16	Charger Control Register 37
0FD8	CHR_CON38	16	Charger Control Register 38
0FDA	CHR_CON39	16	Charger Control Register 39
0FDC	CHR_CON40	16	Charger Control Register 40
0FDE	CHR_CON41	16	Charger Control Register 41
0FE0	CHR_CON42	16	Charger Control Register 42
0FE4	CHR_CON43	16	Charger Control Register 43
0FE6	CHR_CON44	16	Charger Control Register 44

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0FE8	CHR_CON48	16	Charger Control Register 48

0000 **STRUP_CON0 STRUP control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_THR_DET_DIS												
Type				RW												
Reset				0												

Bit(s)	Name	Description
12	RG_THR_DET_DIS	**thermal detection function disable; also disable thermal shut down** 0: normal mode 1: disable thermal detection

0008 **STRUP_CON4 STRUP control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_OSC_EN	JUST_PWRKEY_RST														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
15	DA_QI_OSC_EN	**Internal oscillaotr enable** 0: disable 1: enable
14	JUST_PWRKEY_RST	**Long pressed reset indicator**

000A **STRUP_CON5 STRUP control register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_STRUP_EXT_PMIC_SEL	RG_STRUP_EXT_PMIC_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_STRUP_EXT_PMIC_SEL	**QI_EXT_PMIC_EN control selection** 0: HW mode 1: SW mode
0	RG_STRUP_EXT_PMIC_EN	**QI_EXT_PMIC_EN software mode enable**

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000E **STRUP_CON7** **STRUP control register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**STRUP_PWROFF_SEQ_EN**
Type																RW
Reset																0

Bit(s)	Name	Description
0	STRUP_PWROFF_SEQ_EN	**Power off sequence enable** 0: Disable 1: Enable

001A **STRUP_CON13** **STRUP control register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_STRUP_PWRKEY_COUNT_RESET**
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_STRUP_PWRKEY_COUNT_RESET	**reset the long press shout down counter** 1'b1: reset long press counter 1'b0: no reset long press counter

0024 **STRUP_ANA_CON0** **STRUP_ANA_CON0** **0041**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_FCHR_PU_EN**	**RG_FCHR_KEYDET_EN**	**RG_EN_DRVSEL**	**RG_RST_DRVSEL**	**RG_STRUP_IREF_TRIM**					**RG_VREF_BG**			**RG_THR_TMODE**	**RG_STRUP_THR_SEL**		**RG_THRDET_SEL**
Type	RW	RW	RW	RW	RW					RW			RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Bit(s)	Name	Description
15	RG_FCHR_PU_EN	**FCHR internal resistor pull up enable** 0: disable pull up R 1 : enable pull up R ==> normal key function
14	RG_FCHR_KEYDET_EN	**FCHR mode state hold without key press detection feature** 1 disable

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Bit(s)	Name	Description
		0 enable
13	RG_EN_DRVSEL	**EXT_PMIC_EN pin output driving capability Selection** 0: 7.5mA (default) 1: 15mA
12	RG_RST_DRVSEL	**Reset pin output driving capability Selection** 0: 7.5mA (default) 1: 15mA
11:7	RG_STRUP_IREF_TRIM	**Reference current trimming bits, trimmming current range: 0.5uA~1.4375uA (step=31.25nA), typ=1uA** 00000: 1uA 00001~01111: +31.25nA/step 10000: 0.5uA 10001~11111: +31.25nA/step
6:4	RG_VREF_BG	**Reference current fine tunning to compensate bandgap (BG) voltage variation** 000: VBG=1.16V 001: VBG=1.17V 010: VBG=1.18V 011: VBG=1.19V 100: VBG=1.20V (default) 101: VBG=1.21V 110: VBG=1.22V 111: VBG=1.23V
3	RG_THR_TMODE	**Thermal detection test mode that can measure BJT VEB by input reference voltage of thermal detection comparactor from KPLED** 0: disable 1: enable
2:1	RG_STRUP_THR_SEL	**Thermal shut-down threshold fine tuning** 00 : Initial setting 01 : +5 10 : -5 11 : -10
0	RG_THRDET_SEL	**Thermal detection method selection** 0: four states thermal polling detection 1: three states thermal hysteresis detection method (tranditional detection method)

0026 **STRUP_ANA_CON1** **STRUP_ANA_CON1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_PMU_RSV			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_PMU_RSV	**Reserved bits**

0100 **TYPE_C_PHY_RG_0** **TYPE-C PHY RG 0** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	reg_type_c_phy_rg_cc_mpx_sel									reg_type_c_phy_rg_pd_txslew_i			reg_type_c_phy_rg_pd_tx_slew_calen		type_c_phy_rg_cc_rp_sel	
Type	RW									RW			RW		RW	
Reset	0	0	0	0	0	0	0	0		1	0	0	0		0	0

Bit(s)	Name	Description
15:8	reg_type_c_phy_rg_cc_mpx_sel	**Type-C PHY RG CC mpx select** 8'b0 [NORMAL] 8'b0 [SCAN] 8'b0 [OLT]
6:4	reg_type_c_phy_rg_pd_txslew_i	**Type-C PHY RG PD TX slew rate control code** Default Value: 3'b100 [NORMAL] 3'b100 [SCAN] 3'b100 [OLT]
3	reg_type_c_phy_rg_pd_tx_slew_calen	**Type-C PHY RG PD TX slew rate calibration enable signal** 1: enable 0: disable Default Value: 1'b0 [NORMAL] 1'b0 [SCAN] 1'b0 [OLT]
1:0	type_c_phy_rg_cc_rp_sel	**Type-C PHY RG RP selection of default USB power or 1.5A or 3A** 00: 36K ohm, default USB power 01: 12K ohm, 1.5A 10: 4.7K ohm, 3A 11: reserved Default Value: 2'b00 [NORMAL] 2'b00 [SCAN] 2'b00 [OLT]

0102 **TYPE_C_PHY_RG_CC_RESERVE_CSR** **TYPE-C PHY RG CC Reserve CSR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									reg_type_c_phy_rg_cc_reserve							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	reg_type_c_phy_rg_cc_reserve	**Type-C PHY RG CC reserve** 8'b0 [NORMAL] 8'b0 [SCAN] 8'b0 [OLT]

0104 **TYPE_C_VCMP_CTRL** **TYPE-C Voltage Compare Control** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									reg_type_c_vcmp_dac_en_st_cnt_val	reg_type_c_vcmp_bias_en_st_cnt_val		reg_type_c_vcmp_cc2_sw_sel_st_cnt_val				
Type									RW	RW		RW				
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	reg_type_c_vcmp_dac_en_st_cnt_val	**DAC DA interface adjustment option. Adjust DA_CC_DAC_EN assert cycles before DA_CC_SACLK. Unit: cycles** Default 0. Before 1 cycle.
6:5	reg_type_c_vcmp_bias_en_st_cnt_val	**DAC DA interface adjustment option. Adjust DA_CC_BIAS_EN assert cycles before DA_CC_LPF_EN. Unit: cycles** Default 0. Before 1 cycle.
4:0	reg_type_c_vcmp_cc2_sw_sel_st_cnt_val	**DAC DA interface adjustment option. Adjust DA_CC_SW_SEL assert cycles before DA_CC_SACLK. Unit: cycles** Default 0. Before 1 cycle.

0106 **TYPE_C_CTRL** **TYPE-C Control** **0400**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						reg_type_c_disable_st_rd_en	reg_type_c_attach_src_open_pddebounce_en	reg_type_c_pd2cc_det_disable_en	reg_type_c_attach_src_2_try_wait_snk_st_en	reg_type_c_try_src_st_en	reg_type_c_debug_acc_en	reg_type_c_audio_acc_en	reg_type_c_acc_en	reg_type_c_adc_en	reg_type_c_port_support_role	
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset						1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	reg_type_c_disable_st_rd_en	**Disable state Rd temination enable** 1'b0: Disable. Disable state do not has any terminatiion. 1'b1: Enable. Disable state has Rd terminatiion.
9	reg_type_c_attach_src_open_pddebounce_en	**Attache.SRC detemin SRC.Open voltage use tPDDebounce.** 1'b0: Disable. Without debounce, one time measurement result is valid. 1'b1: Enable. Use tPDDebounce
8	reg_type_c_pd2cc_det_disable_en	**PD 2 CC voltage disable enable. When PD transmission, voltage detection may incorrect.** 1'b0: Enable 1'b1: Disable,
7	reg_type_c_attach_src_2_try_wait_snk_st_en	**Attach.SRC to TryWait.SNK state enable** 1'b0: Disable 1'b1: Enable. Enable Try Attach.SRC to TryWait.SNK state transition.
6	reg_type_c_try_src_st_en	**Try Source state enable** 1'b0: Disable 1'b1: Enable. Enable Try Source state.
5	reg_type_c_debug_ac	**Debug accessory mode enable.**

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Bit(s)	Name	Description
	c_en	1'b0: Disable 1'b1: Enable. Support Debug accessory mode.
4	reg_type_c_audio_acc_en	**Audio accessory mode enable.** 1'b0: Disable 1'b1: Enable. Support Audio accessory mode.
3	reg_type_c_acc_en	**Accessory mode enable.** 1'b0: Disable 1'b1: Enable. Support Accessory mode.
2	reg_type_c_adc_en	**ADC use enable.** 1'b0: Disable 1;b1: Enable. Use ADC detect Rp change in Atrtach.SNK state
1:0	reg_type_c_port_support_role	**Port support role.** 2'b00: Sink 2:b01: Source 2'b10: DRP 2'b11: Reserved

010A **TYPE_C_CC_SW_CTRL** **TYPE-C CC Stoftware Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	w1_type_c_sw_ent_snk_pwr_redetect_cmd			type_c_sw_pd_en	type_c_sw_cc_det_dis	type_c_sw_vbus_det_dis	type_c_sw_da_drive_vconn_en	type_c_sw_vbus_present	w1_type_c_sw_adc_result_met_vrd_30_cmd	w1_type_c_sw_adc_result_met_vrd_15_cmd	w1_type_c_sw_adc_result_met_vrd_default_cmd	w1_type_c_sw_vconn_swap_indicate_cmd	w1_type_c_sw_pr_swap_indicate_cmd	w1_type_c_sw_ent_unatch_snk_cmd	w1_type_c_sw_ent_unatch_src_cmd	w1_type_c_sw_ent_disable_cmd
Type	WO			RW	RW	RW	RW	RW	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	w1_type_c_sw_ent_snk_pwr_redetect_cmd	**Type-C software enter Sink power redetect state command. Valid when Sink power sub-state not in Idle state.**
12	type_c_sw_pd_en	**Type-C software Power delivery enable** 1'b0: Disable 1'b1: Enable. Desgin will enable DA_PD_BIAS_EN & DA_PD_CC_SW[1] & met timing spec.
11	type_c_sw_cc_det_dis	**Type-C software CC detection disable.** 1'b0: Enable 1'b1: Disable CC detection. Voltage compare will not trigger.
10	type_c_sw_vbus_det_dis	**Type-C software VBUS detection disable.** 1'b0: Enable 1'b1: Disable VBUS detection. Ignore VBUS detection result.
9	type_c_sw_da_drive_vconn_en	**Type-C software drive VCONN enable** 1'b0: Disable 1'b1: Enable
8	type_c_sw_vbus_present	**Type-C software VBUS present.** 0: VBUS not present 1: VBUS present
7	w1_type_c_sw_adc_r	**Type-C software ADC result met snk.vrd30. Valid when reg_adc_en**

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Bit(s)	Name	Description
	esult_met_vrd_30_cmd	**= 1'b1**
6	w1_type_c_sw_adc_result_met_vrd_15_cmd	**Type-C software ADC result met snk.vrd15. Valid when reg_adc_en = 1'b1**
5	w1_type_c_sw_adc_result_met_vrd_default_cmd	**Type-C software ADC result met snk.vrddefault. Valid when reg_adc_en = 1'b1**
4	w1_type_c_sw_vconn_swap_indicate_cmd	**Type-C software indicate VCONN_SWAP command, Write 1 to inform VCONN_SWAP is done.**
3	w1_type_c_sw_pr_swap_indicate_cmd	**Type-C software indicate PR_SWAP command, Write 1 to inform PR_SWAP is done.** Then CC deisng will change state if current is in attach.src or attach.snk.
2	w1_type_c_sw_ent_unatch_snk_cmd	**Type-C software enter unatach Sink state command**
1	w1_type_c_sw_ent_unatch_src_cmd	**Type-C software enter unatach Source state command**
0	w1_type_c_sw_ent_disable_cmd	**Type-C software enter disable state command**

010C **TYPE_C_CC_VOL_PERIODIC_MEAS_VAL** **TYPE-C CC Voltage Periodic Measure Value** **02ED**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_cc_vol_periodic_meas_val												
Type				RW												
Reset				0	0	0	1	0	1	1	1	0	1	1	0	1

Bit(s)	Name	Description
12:0	reg_type_c_cc_vol_periodic_meas_val	**Type-C CC voltage periodic measure value** Every (periodic measure value) cycle counts will trigger one voltage measure event. Not to over 15ms. 15ms is the minimum time tha DRP stay in certain unattach state. Not to smaller than 1ms. Make sure to measure stable voltage after cc termination is changed. Default set 10ms. Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (750 -1).

010E **TYPE_C_CC_VOL_DEBOUCE_CNT_VAL** **TYPE-C CC Voltage Debounce Count Value** **020A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_cc_vol_pd_debounce_cnt_val					reg_type_c_cc_vol_cc_debounce_cnt_val							
Type				RW					RW							
Reset				0	0	0	1	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
12:8	reg_type_c_cc_vol_pd_debounce_cnt_val	**Type-C CC Voltage PD debounce count value** PD deounce time met when voltage measurement result is the same for PD debounce counts. tCCDebounce: 10ms ~ 20ms Set value = (tPDDebounce/(type_c_cc_vcomp_periodic_meas_val +1)) Use 20ms & suppose measure period is 10ms. Default set to 2
7:0	reg_type_c_cc_vol_cc_debounce_cnt_val	**Type-C CC Voltage CC debounce count value** CC deounce time met when voltage measurement result is the same for CC debounce counts. tCCDebounce: 100ms ~ 200ms Set value = (tCCDebounce/(type_c_cc_vcomp_periodic_meas_val+1) Use 100ms & suppose measure period is 10ms. Default set to 10

0110 **TYPE_C_DRP_SRC_CNT_VAL_0** **TYPE-C DRP Source Count Value 0** **0EA5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_drp_src_cnt_val_0															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	0	1	0	0	1	0	1

Bit(s)	Name	Description
15:0	reg_type_c_drp_src_cnt_val_0	**Type-C DRP Source count value 0** The time that DRP stay in Unattached.SRC state. Indicate type_c_drp_src_cnt_val[15:0] Default set 50ms. Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (3750 -1).

0114 **TYPE_C_DRP_SNK_CNT_VAL_0** **TYPE-C DRP Sink Count Value 0** **0EA5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_drp_snk_cnt_val_0															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	0	1	0	0	1	0	1

Bit(s)	Name	Description
15:0	reg_type_c_drp_snk_cnt_val_0	**Type-C DRP Sink count value 0** The time that DRP stay in Unattached.SNK state. Indicate type_c_drp_snk_cnt_val[15:0] Spec 50~100ms Default use 50ms Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (3750 -1).

0118 **TYPE_C_DRP_TRY_CNT_V** **TYPE-C DRP Try Count Value 0** **1D4B**

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AL_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_drp_try_cnt_val_0															
Type	RW															
Reset	0	0	0	1	1	1	0	1	0	1	0	0	1	0	1	1

Bit(s)	Name	Description
15:0	reg_type_c_drp_try_cnt_val_0	**Type-C DRP Try count value 0** The time that DRP stay in Try.SRC state. Indicate type_c_drp_try_cnt_val[15:0] Spec 75~150ms Default use 100ms Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (7500 -1).

011C	TYPE_C_DRP_TRY_WAIT_CNT_VAL_0	TYPE-C DRP Try Wait Count Value 0	752F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_drp_try_wait_cnt_val_0															
Type	RW															
Reset	0	1	1	1	0	1	0	1	0	0	1	0	1	1	1	1

Bit(s)	Name	Description
15:0	reg_type_c_drp_try_wait_cnt_val_0	**Type-C DRP Try Wait count value 0** The time that DRP stay in TryWait.SNK state. Indicate type_c_drp_try_wait_cnt_val[15:0] Spec 400~800ms Default use 400ms Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (30000 -1).

011E	TYPE_C_DRP_TRY_WAIT_CNT_VAL_1	TYPE-C DRP Try Wait Count Value 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													reg_type_c_drp_try_wait_cnt_val_1			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	reg_type_c_drp_try_wait_cnt_val_1	**Type-C DRP Try Wait count value 1** The time that DRP stay in TryWait.SNK state. Indicate type_c_drp_try_wait_cnt_val[19:16] Spec 400~800ms Default use 400ms Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (30000 -1).

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0120	TYPE_C_CC_SRC_DEFAULT_DAC_VAL	TYPE-C CC SRC Default DAC Value	0225

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_cc_src_vrd_default_dac_val								reg_type_c_cc_src_vopen_default_dac_val					
Type			RW								RW					
Reset			0	0	0	0	1	0			1	0	0	1	0	1

Bit(s)	Name	Description
13:8	reg_type_c_cc_src_vrd_default_dac_val	**Type-C CC Source VRD default DAC value** The value to for DAC to compare Source VRD voltage when support default current
5:0	reg_type_c_cc_src_vopen_default_dac_val	**Type-C CC Source VOPEN default DAC value** The value to for DAC to compare Source VOPEN voltage when support default current

0122	TYPE_C_CC_SRC_15_DAC_VAL	TYPE-C CC SRC 15 DAC Value	0725

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_cc_src_vrd_15_dac_val								reg_type_c_cc_src_vopen_15_dac_val					
Type			RW								RW					
Reset			0	0	0	1	1	1			1	0	0	1	0	1

Bit(s)	Name	Description
13:8	reg_type_c_cc_src_vrd_15_dac_val	**Type-C CC Source VRD 15 DAC value** The value to for DAC to compare Source VRD voltage when support 1.5A current
5:0	reg_type_c_cc_src_vopen_15_dac_val	**Type-C CC Source VOPEN 15 DAC value** The value to for DAC to compare Source VOPEN voltage when support 1.5A current

0124	TYPE_C_CC_SRC_30_DAC_VAL	TYPE-C CC SRC 30 DAC Value	113E

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_cc_src_vrd_30_dac_val								reg_type_c_cc_src_vopen_30_dac_val					
Type			RW								RW					
Reset			0	1	0	0	0	1			1	1	1	1	1	0

Bit(s)	Name	Description
13:8	reg_type_c_cc_src_vrd_30_dac_val	**Type-C CC Source VRD 30 DAC value** The value to for DAC to compare Source VRD voltage when support 3.0A current
5:0	reg_type_c_cc_src_vopen_30_dac_val	**Type-C CC Source VOPEN 30 DAC value** The value to for DAC to compare Source VOPEN voltage when support 3.0A

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Bit(s)	Name	Description
		current

0128 **TYPE_C_CC_SNK_DAC_VAL_0** **TYPE-C CC SNK DAC Value 0** **0E1D**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_cc_snk_vrp15_dac_val								reg_type_c_cc_snk_vrp30_dac_val					
Type			RW								RW					
Reset			0	0	1	1	1	0			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	reg_type_c_cc_snk_vrp15_dac_val	**Type-C CC Sink VRP15 DAC value** The value to for DAC to compare Sink VRP15 voltage
5:0	reg_type_c_cc_snk_vrp30_dac_val	**Type-C CC Sink VRP30 DAC value** The value to for DAC to compare Sink VRP30 voltage

012A **TYPE_C_CC_SNK_DAC_VAL_1** **TYPE-C CC SNK DAC Value 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											reg_type_c_cc_snk_vrpusb_dac_val					
Type											RW					
Reset											0	0	0	0	1	0

Bit(s)	Name	Description
5:0	reg_type_c_cc_snk_vrpusb_dac_val	**Type-C CC Sink VRPUSB DAC value** The value to for DAC to compare Sink VRPUSB voltage

0130 **TYPE_C_INTR_EN_0** **TYPE-C Interrupt Enable 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_cc_ent_attach_wait_acc_intr_en	reg_type_c_cc_ent_unattach_acc_intr_en	reg_type_c_cc_ent_try_wait_snk_intr_en	reg_type_c_cc_ent_try_src_intr_en	reg_type_c_cc_ent_attach_wait_snk_intr_en	reg_type_c_cc_ent_attach_wait_src_intr_en	reg_type_c_cc_ent_unattach_snk_intr_en	reg_type_c_cc_ent_unattach_src_intr_en	reg_type_c_cc_ent_disable_intr_en	reg_type_c_cc_ent_dbg_acc_intr_en	reg_type_c_cc_ent_audio_acc_intr_en	reg_type_c_cc_ent_attach_snk_intr_en	reg_type_c_cc_ent_attach_src_intr_en
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	reg_type_c_cc_ent_attach_wait_acc_intr_en	**Type-C CC enter AttachWait.Accessory state interrupt enable.** Enable type_c_cc_ent_attach_wait_acc_intr interrupt.

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Bit(s)	Name	Description
11	reg_type_c_cc_ent_unattach_acc_intr_en	**Type-C CC enter Unattach.Accessory state interrupt enable.** Enable type_c_cc_ent_unattach_acc_intr interrupt.
10	reg_type_c_cc_ent_try_wait_snk_intr_en	**Type-C CC enter TryWait.SNK state interrupt enable.** Enable interrupt.
9	reg_type_c_cc_ent_try_src_intr_en	**Type-C CC enter Try.SRC state interrupt enable.** Enable type_c_cc_ent_try_src_intr interrupt.
8	reg_type_c_cc_ent_attach_wait_snk_intr_en	**Type-C CC enter AttachWait.SNK state interrupt enable.** Enable type_c_cc_ent_attach_wait_snk_intr interrupt.
7	reg_type_c_cc_ent_attach_wait_src_intr_en	**Type-C CC enter AttachWait.SRC state interrupt enable.** Enable type_c_cc_ent_attach_wait_src_intr interrupt.
6	reg_type_c_cc_ent_unattach_snk_intr_en	**Type-C CC enter Unattach.SNK state interrupt enable.** Enable type_c_cc_ent_unattach_snk_intr interrupt.
5	reg_type_c_cc_ent_unattach_src_intr_en	**Type-C CC enter Unattach.SRC state interrupt enable.** Enable type_c_cc_ent_unattach_src_intr interrupt.
4	reg_type_c_cc_ent_disable_intr_en	**Type-C CC enter Disable state interrupt enable.** Enable type_c_cc_ent_disable_intr interrupt.
3	reg_type_c_cc_ent_dbg_acc_intr_en	**Type-C CC enter debug accessory interrupt enable.** Enable type_c_cc_ent_debug_acc_intr interrupt.
2	reg_type_c_cc_ent_audio_acc_intr_en	**Type-C CC enter audio accessory interrupt enable.** Enable type_c_cc_ent_audio_acc_intr interrupt.
1	reg_type_c_cc_ent_attach_snk_intr_en	**Type-C CC enter attach Sink interrupt enable.** Enable type_c_cc_ent_attach_snk_intr interrupt.
0	reg_type_c_cc_ent_attach_src_intr_en	**Type-C CC enter attach Source interrupt enable.** Enable type_c_cc_ent_attach_src_intr interrupt.

0134 **TYPE_C_INTR_EN_2** **TYPE-C Interrupt Enable 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												reg_type_c_cc_ent_snk_pwr_redetect_intr_en	reg_type_c_cc_ent_snk_pwr_30_intr_en	reg_type_c_cc_ent_snk_pwr_15_intr_en	reg_type_c_cc_ent_snk_pwr_default_intr_en	reg_type_c_cc_ent_snk_pwr_idle_intr_en
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	reg_type_c_cc_ent_snk_pwr_redetect_intr_en	**Type-C CC enter sink power redetect current sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_redetect interrupt.
3	reg_type_c_cc_ent_snk_pwr_30_intr_en	**Type-C CC enter sink power 3.0A current sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_30 interrupt.
2	reg_type_c_cc_ent_snk_pwr_15_intr_en	**Type-C CC enter sink power 1.5A current sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_15 interrupt.

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Bit(s)	Name	Description
1	reg_type_c_cc_ent_snk_pwr_default_intr_en	**Type-C CC enter sink power default current sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_default interrupt.
0	reg_type_c_cc_ent_snk_pwr_idle_intr_en	**Type-C CC enter sink power idle sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_idle interrupt.

0138 **TYPE_C_INTR_0** **TYPE-C Interrupt 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				type_c_cc_ent_attach_wait_acc_intr	type_c_cc_ent_unattach_acc_intr	type_c_cc_ent_try_wait_snk_intr	type_c_cc_ent_try_src_intr	type_c_cc_ent_attach_wait_snk_intr	type_c_cc_ent_attach_wait_src_intr	type_c_cc_ent_unattach_snk_intr	type_c_cc_ent_unattach_src_intr	type_c_cc_ent_disable_intr	type_c_cc_ent_dbg_acc_intr	type_c_cc_ent_audio_acc_intr	type_c_cc_ent_attach_snk_intr	type_c_cc_ent_attach_src_intr
Type				W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	type_c_cc_ent_attach_wait_acc_intr	**Type-C CC enter AttachWait.Accessory state interrupt.** Set when CC enter AttachWait.Accessory state.
11	type_c_cc_ent_unattach_acc_intr	**Type-C CC enter Unattach.Accessory state interrupt.** Set when CC enter Unattach.Accessory state.
10	type_c_cc_ent_try_wait_snk_intr	**Type-C CC enter TryWait.SNK state interrupt.** Set when CC enter TryWait.SNK state.
9	type_c_cc_ent_try_src_intr	**Type-C CC enter Try.SRC state interrupt.** Set when CC enter Try.SRC state.
8	type_c_cc_ent_attach_wait_snk_intr	**Type-C CC enter AttachWait.SNK state interrupt.** Set when CC enter AttachWait.SNK state.
7	type_c_cc_ent_attach_wait_src_intr	**Type-C CC enter AttachWait.SRC state interrupt.** Set when CC enter AttachWait.SRC state.
6	type_c_cc_ent_unattach_snk_intr	**Type-C CC enter Unattach.SNK state interrupt.** Set when CC enter Unattaach.SNK state.
5	type_c_cc_ent_unattach_src_intr	**Type-C CC enter Unattach.SRC state interrupt.** Set when CC enter Unattach.SRC state.
4	type_c_cc_ent_disable_intr	**Type-C CC enter Disable state interrupt.** Set when CC enter Disable state.
3	type_c_cc_ent_dbg_acc_intr	**Type-C CC enter DebugAccessory state interrupt.** Set when CC enter DebugAccessory state.
2	type_c_cc_ent_audio_acc_intr	**Type-C CC enter AudioAccessory state interrupt.** Set when CC enter AudioAccessory state.
1	type_c_cc_ent_attach_snk_intr	**Type-C CC enter Attach.SNK state interrupt.** Set when CC enter Attach.SNK state.
0	type_c_cc_ent_attach_src_intr	**Type-C CC enter Attach.SRC state interrupt.** Set when CC enter Attach.SRC state.

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013C	TYPE_C_INTR_2	TYPE-C Interrupt 2	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												type_c_cc_ent_snk_pwr_redetect_intr	type_c_cc_ent_snk_pwr_30_intr	type_c_cc_ent_snk_pwr_15_intr	type_c_cc_ent_snk_pwr_default_intr	type_c_cc_ent_snk_pwr_idle_intr
Type												W1C	W1C	W1C	W1C	W1C
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	type_c_cc_ent_snk_pwr_redetect_intr	**Type-C CC enter sink power redetect current state inerrupt** Set when enter Redetect.SNK state.
3	type_c_cc_ent_snk_pwr_30_intr	**Type-C CC enter sink power 3.0A current state inerrupt** Set when enter Power3.0.SNK state.
2	type_c_cc_ent_snk_pwr_15_intr	**Type-C CC enter sink power 1.5A current state inerrupt** Set when enter Power1.5.SNK state.
1	type_c_cc_ent_snk_pwr_default_intr	**Type-C CC enter sink power default current state inerrupt** Set when enter PowerDefault.SNK state.
0	type_c_cc_ent_snk_pwr_idle_intr	**Type-C CC enter sink power idle state inerrupt** Set when enter Sink Power Idle state.

0140	TYPE_C_CC_STATUS	TYPE-C CC Status	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ro_type_c_routed_cc												ro_type_c_cc_st			
Type	RU												RU			
Reset	0												0	0	0	0

Bit(s)	Name	Description
15	ro_type_c_routed_cc	**Type-C routed CC** 1'b0: cc1 1'b1: cc2
3:0	ro_type_c_cc_st	**Type-C CC state.** 4'd0: Disable 4'd1: Unattached Source 4'd2: Attach Wait Source 4'd3: Attach Source 4'd4: Unatched Sink 4'd5: Attach Wait Sink 4'd6: Attach Sink 4'd7: Try Source 4'd8: Try Wait Sink 4'd9: Unattached Accessory 4'd10: Attach Wait Accessory 4'd11: Audio Accessory 4'd12: Debug Accessory

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Bit(s)	Name	Description
		Others: Unused

0142 **TYPE_C_PWR_STATUS** **TYPE-C Power Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ro_ad_cc_vusb33_rdy	ro_type_c_ad_cc_cmp_out	ro_type_c_drive_vconn_capable	ro_type_c_cc_pwr_role		ro_type_c_cc_snk_pwr_st		
Type									RU	RU	RU	RU		RU		
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7	ro_ad_cc_vusb33_rdy	**AD CC VUSB33 ready** 1'b0: VUSB33 not ready yet 1'b1: VUSB33 ready Default value depends on current VUSB33 status
6	ro_type_c_ad_cc_cmp_out	**Type-C AD comprator output result** 1'b0: CC voltage < DAC out 1'b1: CC voltage > DAC out
5	ro_type_c_drive_vconn_capable	**Type-C capable to drive VCONN** 1'b0: Can not drive 1'b1: Can drive According to SPEC, first attach Source a. Drive Vconn when other CC pin in SRC.Ra for tCCDebounce. SW must read this CSR before drive VCONN b. Drive Vconn unconditionaly. SW no need to read this CSR.
4	ro_type_c_cc_pwr_role	**Type-C power role.** 1'b0: Sink 1'b1: Source
2:0	ro_type_c_cc_snk_pwr_st	**Type-C Sink power state.** 3'd0: Sink Power Idle 3'd1: Sink Power Defaule 3'd2: Sink Power 1.5A 3'd3: Sink Power 3.0A 3'd3: Sink Power redetect

0144 **TYPE_C_PHY_RG_CC1_RESISTENCE_0** **TYPE-C PHY RG CC1 Resistence_0** **1004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_phy_rg_cc1_rp15										reg_type_c_phy_rg_cc1_rpde		
Type				RW										RW		
Reset				1	0	0	0	0						1	0	0

Bit(s)	Name	Description
12:8	reg_type_c_phy_rg_cc1_rp15	**Type-C PHY RG CC1 1.5A Rp control code.** Default value:

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Bit(s)	Name	Description
		5'b10000 [NORMAL] 5'b10000 [SCAN] 5'b10000 [OLT]
2:0	reg_type_c_phy_rg_cc1_rpde	**Type-C PHY RG CC1 default current Rp control code.** Default value: 3'b100 [NORMAL] 3'b100 [SCAN] 3'b100 [OLT]

0146 **TYPE_C_PHY_RG_CC1_RESISTENCE_1** **TYPE-C PHY RG CC1 Resistence_1** **1010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_phy_rg_cc1_rd								reg_type_c_phy_rg_cc1_rp3				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
12:8	reg_type_c_phy_rg_cc1_rd	**Type-C PHY RG CC1 Rd control code.** Default value: 5'b10000 [NORMAL] 5'b10000 [SCAN] 5'b10000 [OLT]
4:0	reg_type_c_phy_rg_cc1_rp3	**Type-C PHY RG CC1 3.0A Rp control code.** Default value: 5'b10000 [NORMAL] 5'b10000 [SCAN] 5'b10000 [OLT]

0148 **TYPE_C_PHY_RG_CC2_RESISTENCE_0** **TYPE-C PHY RG CC2 Resistence_0** **1004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_phy_rg_cc2_rp15										reg_type_c_phy_rg_cc2_rpde		
Type				RW										RW		
Reset				1	0	0	0	0						1	0	0

Bit(s)	Name	Description
12:8	reg_type_c_phy_rg_cc2_rp15	**Type-C PHY RG CC2 1.5A Rp control code.** Default value: 5'b10000 [NORMAL] 5'b10000 [SCAN] 5'b10000 [OLT]
2:0	reg_type_c_phy_rg_cc2_rpde	**Type-C PHY RG CC2 default Rp control code.** Default value: 3'b100 [NORMAL] 3'b100 [SCAN] 3'b100 [OLT]

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014A	TYPE_C_PHY_RG_CC2_RESISTENCE_1	TYPE-C PHY RG CC2 Resistence_1	1010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_phy_rg_cc2_rd								reg_type_c_phy_rg_cc2_rp3				
Type				RW								RW				
Reset				1	0	0	0	0				1	0	0	0	0

Bit(s)	Name	Description
12:8	reg_type_c_phy_rg_cc2_rd	**Type-C PHY RG CC2 Rd control code.** Default value: 5'b10000 [NORMAL] 5'b10000 [SCAN] 5'b10000 [OLT]
4:0	reg_type_c_phy_rg_cc2_rp3	**Type-C PHY RG CC2 3.0A Rp control code.** Default value: 5'b10000 [NORMAL] 5'b10000 [SCAN] 5'b10000 [OLT]

0160	TYPE_C_CC_SW_FORCE_MODE_ENABLE	TYPE-C CC SW Force Mode Enable	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_sw_force_mode_en_da_cc_dac_gain_cal	reg_type_c_sw_force_mode_en_da_cc_dac_cal	reg_type_c_sw_force_mode_en_da_cc_dac_in	reg_type_c_sw_force_mode_en_da_cc_saclk	reg_type_c_sw_force_mode_en_da_cc_dac_en	reg_type_c_sw_force_mode_en_da_cc_sacsw_en	reg_type_c_sw_force_mode_en_da_cc_adcsw_en	reg_type_c_sw_force_mode_en_da_cc_lpf_en	reg_type_c_sw_force_mode_en_da_cc_bias_en	reg_type_c_sw_force_mode_en_da_cc_sw_sel	reg_type_c_sw_force_mode_en_da_cc_lev_en	reg_type_c_sw_force_mode_en_da_cc_rc2	reg_type_c_sw_force_mode_en_da_cc_rc1
Type				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	reg_type_c_sw_force_mode_en_da_cc_dac_gain_cal	**Software force mode enable for DA_CC_DAC_GAIN_CAL** 1'b0: Disable. 1'b1: Enable. DA_CC_DAC_GAIN_CAL = type_c_sw_force_mode_da_cc_dac_gain_cal
11	reg_type_c_sw_force_mode_en_da_cc_dac_cal	**Software force mode enable for DA_CC_DAC_CAL** 1'b0: Disable. 1'b1: Enable. DA_CC_DAC_CAL = type_c_sw_force_mode_da_cc_dac_cal
10	reg_type_c_sw_force_mode_en_da_cc_dac_in	**Software force mode enable for DA_CC_DAC_IN** 1'b0: Disable. 1'b1: Enable. DA_CC_DAC_IN = type_c_sw_force_mode_da_cc_dac_in
9	reg_type_c_sw_force_mode_en_da_cc_saclk	**Software force mode enable for DA_CC_SACLK** 1'b0: Disable. 1'b1: Enable.

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Bit(s)	Name	Description
		DA_CC_SACLK = type_c_sw_force_mode_en_da_cc_saclk
8	reg_type_c_sw_force_mode_en_da_cc_dac_en	**Software force mode enable for DA_CC_DAC_EN** 1'b0: Disable. 1'b1: Enable. DA_CC_DAC_EN = type_c_sw_force_mode_da_cc_dac_en
7	reg_type_c_sw_force_mode_en_da_cc_sasw_en	**Software force mode enable for DA_CC_SASW_EN** 1'b0: Disable. 1'b1: Enable. DA_CC_SASW_EN = type_c_sw_force_mode_en_da_cc_sasw_en
6	reg_type_c_sw_force_mode_en_da_cc_adcsw_en	**Software force mode enable for DA_CC_ADCSW_EN** 1'b0: Disable. 1'b1: Enable. DA_CC_ADCSW_EN = type_c_sw_force_mode_da_cc_adcsw_en
5	reg_type_c_sw_force_mode_en_da_cc_lpf_en	**Software force mode enable for DA_CC_LPF_EN** 1'b0: Disable. 1'b1: Enable. DA_CC_LPF_EN = type_c_sw_force_mode_da_cc_lpf_en
4	reg_type_c_sw_force_mode_en_da_cc_bias_en	**Software force mode enable for DA_CC_BIAS_EN** 1'b0: Disable. 1'b1: Enable. DA_CC_BIAS_EN = type_c_sw_force_mode_da_cc_bias_en
3	reg_type_c_sw_force_mode_en_da_cc_sw_sel	**Software force mode enable for DA_CC_SW_SEL** 1'b0: Disable. 1'b1: Enable. DA_CC_SW_SEL= type_c_sw_force_mode_da_cc_w_sel
2	reg_type_c_sw_force_mode_en_da_cc_lev_en	**Software force mode enable for DA_CC_LEV_EN** 1'b0: Disable. 1'b1: Enable. DA_CC_LEV_EN = type_c_sw_force_mode_da_cc_lev_en
1	reg_type_c_sw_force_mode_en_da_cc_rcc2	**Software force mode enable for CC2 termination** 1'b0: Disable. 1'b1: Enable. DA_CC_RPCC2_EN = type_c_sw_force_mode_da_cc_rpcc2_en DA_CC_RDCC2_EN = type_c_sw_force_mode_da_cc_rdcc2_en DA_CC_RACC2_EN = type_c_sw_force_mode_da_cc_racc2_en
0	reg_type_c_sw_force_mode_en_da_cc_rcc1	**Software force mode enable for CC1 termination** 1'b0: Disable. 1'b1: Enable. DA_CC_RPCC1_EN = type_c_sw_force_mode_da_cc_rpcc1_en DA_CC_RDCC1_EN = type_c_sw_force_mode_da_cc_rdcc1_en DA_CC_RACC1_EN = type_c_sw_force_mode_da_cc_racc1_en

0164 **TYPE_C_CC_SW_FORCE_MODE_VAL_0** **TYPE-C CC SW Force Mode Value_0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_sw_force_mode_da_cc_saclk	reg_type_c_sw_force_mode_da_cc_dac_en	reg_type_c_sw_force_mode_da_cc_sasw_	reg_type_c_sw_force_mode_da_cc_adcsw	reg_type_c_sw_force_mode_da_cc_lpf_en	reg_type_c_sw_force_mode_da_cc_bias_e	reg_type_c_sw_force_mode_da_cc_sw_sel	reg_type_c_sw_force_mode_da_cc_lev_en	reg_type_c_sw_force_mode_da_cc_racc2_	reg_type_c_sw_force_mode_da_cc_rdcc2_	reg_type_c_sw_force_mode_da_cc_rpcc2_en	reg_type_c_sw_force_mode_da_cc_racc1_	reg_type_c_sw_force_mode_da_cc_rdcc1_	reg_type_c_sw_force_mode_da_cc_rpcc1_

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					en	**_en**		**n**			**en**	**en**		**en**	**en**	**en**
Type			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	reg_type_c_sw_force_mode_da_cc_saclk	**Software force mode enable for DA_CC_SACLK**
12	reg_type_c_sw_force_mode_da_cc_dac_en	**Software force mode enable for DA_CC_DAC_EN**
11	reg_type_c_sw_force_mode_da_cc_sasw_en	**Software force mode enable for DA_CC_SASW_EN**
10	reg_type_c_sw_force_mode_da_cc_adcsw_en	**Software force mode enable for DA_CC_ADCSW_EN**
9	reg_type_c_sw_force_mode_da_cc_lpf_en	**Software force mode enable for DA_CC_LPF_EN**
8	reg_type_c_sw_force_mode_da_cc_bias_en	**Software force mode enable for DA_CC_BIAS_EN**
7	reg_type_c_sw_force_mode_da_cc_sw_sel	**Software force mode enable for DA_CC_SW_SEL**
6	reg_type_c_sw_force_mode_da_cc_lev_en	**Software force mode enable for DA_CC_LEV_EN**
5	reg_type_c_sw_force_mode_da_cc_racc2_en	**Software force mode enable for DA_CC_RACC2_EN**
4	reg_type_c_sw_force_mode_da_cc_rdcc2_en	**Software force mode enable for DA_CC_RDCC2_EN**
3	reg_type_c_sw_force_mode_da_cc_rpcc2_en	**Software force mode enable for DA_CC_RPCC2_EN**
2	reg_type_c_sw_force_mode_da_cc_racc1_en	**Software force mode enable for DA_CC_RACC1_EN**
1	reg_type_c_sw_force_mode_da_cc_rdcc1_en	**Software force mode enable for DA_CC_RDCC1_EN**
0	reg_type_c_sw_force_mode_da_cc_rpcc1_en	**Software force mode enable for DA_CC_RPCC1_EN**

0166 **TYPE_C_CC_SW_FORCE_MODE_VAL_1** **TYPE-C CC SW Force Mode Value_1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**reg_type_c_sw_force_mode_da_cc_dac_gain_cal**				**reg_type_c_sw_force_mode_da_cc_dac_cal**						**reg_type_c_sw_force_mode_da_cc_dac_in**					
Type	RW				RW						RW					
Reset	0	0	0	0	0	0	0	0			0	0	0	0	0	0

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Bit(s)	Name	Description
15:12	reg_type_c_sw_force_mode_da_cc_dac_gain_cal	**Software force mode enable for DA_CC_DAC_GAIN_CAL**
11:8	reg_type_c_sw_force_mode_da_cc_dac_cal	**Software force mode enable for DA_CC_DAC_CAL**
5:0	reg_type_c_sw_force_mode_da_cc_dac_in	**Software force mode enable for DA_CC_DAC_IN**

0170 **TYPE_C_CC_DAC_CALI_CTRL** **TYPE-C CC DAC Calibration Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ro_type_c_dac_fail	ro_type_c_dac_ok			reg_type_c_dac_cal_stage	type_c_dac_cal_start
Type											RU	RU			RW	RW
Reset											0	0			0	0

Bit(s)	Name	Description
5	ro_type_c_dac_fail	**DAC calibration fail flag.** Set when DAC calibration fail. Clear when set type_c_dac_cal_start = 1'b0
4	ro_type_c_dac_ok	**DAC calibration done flag.** Set when DAC calibration done. Clear when set type_c_dac_cal_start = 1'b0
1	reg_type_c_dac_cal_stage	**1'b0: 1st stage. da_cc_dac_cal & da_cc_dac_gain_cal** 1'b1: 2nd stage. da_cc_dac_gain_cal
0	type_c_dac_cal_start	**Set 1'b1 to start the DAC calibration.**

0172 **TYPE_C_CC_DAC_CALI_RESULT** **TYPE-C CC DAC Calibration Result** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ro_da_cc_dac_gain_cal				ro_da_cc_dac_cal			
Type									RU				RU			
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:4	ro_da_cc_dac_gain_cal	**Read update register. Save calibration result of DA_CC_GAIN_DAC_CAL.**
3:0	ro_da_cc_dac_cal	**Read update register. Save calibration result of DA_CC_DAC_CAL.**

0180 **TYPE_C_DEBUG_PORT_SE** **Debug Port Select 0** **0000**

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LECT_0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_dbg_port_sel_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	reg_type_c_dbg_port_sel_0	**Type-c PD debud port select 0** [7:0] selection of debug port[7:0] [15:8] selection of debug port[15:8]

0182 TYPE_C_DEBUG_PORT_SELECT_1 Debug Port Select 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_dbg_port_sel_1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	reg_type_c_dbg_port_sel_1	**Type-c PD debud port select 1** [7:0] selection of debug port[23:16] [15:8] selection of debug port[31:24]

0184 TYPE_C_DEBUG_MODE_SELECT Debug Mode Select 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_dbg_mod_sel															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	reg_type_c_dbg_mod_sel	**Type-c PD debud mode select** [3:0] selection of debug port[7:0] [7:4] selection of debug port[15:8] [11:8] selection of debug port[23:16] [15:12] selection of debug port[31:24] 4'b0: select cc debug signal 4'b1: select pd debug signal

0188 TYPE_C_DEBUG_OUT_READ_0 Debug Out Read 0 0101

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ro_type_c_dbg_out_read_0															
Type	RU															

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Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	ro_type_c_dbg_out_read_0	**Type-c PD debud mode select** [3:0] selection of debug port[7:0] [7:4] selection of debug port[15:8] [11:8] selection of debug port[23:16] [15:12] selection of debug port[31:24] 4'b0: select pd debug signal 4'b1: select type-c debug signal

018A **TYPE_C_DEBUG_OUT_READ_1** **Debug Out Read 1** **0101**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ro_type_c_dbg_out_read_1															
Type	RU															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	ro_type_c_dbg_out_read_1	**Type-c PD debud mode select** [3:0] selection of debug port[7:0] [7:4] selection of debug port[15:8] [11:8] selection of debug port[23:16] [15:12] selection of debug port[31:24] 4'b0: select pd debug signal 4'b1: select type-c debug signal

0206 **TEST_OUT** **TEST_OUT** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TEST_OUT							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TEST_OUT	**Monitor**

020E **EN_STATUS1** **Regulator status 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_STATUS_VTCXO28	EN_STATUS_VTCXO24	EN_STATUS_VXO22	EN_STATUS_VRF18	EN_STATUS_VRF12	EN_STATUS_VCN33	EN_STATUS_VCN28	EN_STATUS_VCN18	EN_STATUS_VCAMA	EN_STATUS_VCAMIO	EN_STATUS_VLDO28	EN_STATUS_VCAMD	EN_STATUS_VAUX18	EN_STATUS_VAUD28	EN_STATUS_VSRAM_PROC	EN_STATUS_VDRAM
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	EN_STATUS_VTCXO28	0: off 1: on
14	EN_STATUS_VTCXO24	0: off 1: on
13	EN_STATUS_VXO22	0: off 1: on
12	EN_STATUS_VRF18	0: off 1: on
11	EN_STATUS_VRF12	0: off 1: on
10	EN_STATUS_VCN33	0: off 1: on
9	EN_STATUS_VCN28	0: off 1: on
8	EN_STATUS_VCN18	0: off 1: on
7	EN_STATUS_VCAMA	0: off 1: on
6	EN_STATUS_VCAMIO	0: off 1: on
5	EN_STATUS_VLDO28	0: off 1: on
4	EN_STATUS_VCAMD	0: off 1: on
3	EN_STATUS_VAUX18	0: off 1: on
2	EN_STATUS_VAUD28	0: off 1: on
1	EN_STATUS_VSRAM_PROC	0: off 1: on
0	EN_STATUS_VDRAM	0: off 1: on

0210 EN_STATUS2 Regulator status 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_STATUS_VSIM1	EN_STATUS_VSIM2	EN_STATUS_VIO28	EN_STATUS_VMC	EN_STATUS_VMCH	EN_STATUS_VUSB33	EN_STATUS_VEMC33	EN_STATUS_VIO18	EN_STATUS_VIBR	EN_STATUS_TREF	EN_STATUS_VRTC	EN_STATUS_VPA	EN_STATUS_VPROC	EN_STATUS_VCORE	EN_STATUS_VS1	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
15	EN_STATUS_VSIM1	0: off 1: on
14	EN_STATUS_VSIM2	0: off 1: on
13	EN_STATUS_VIO28	0: off 1: on
12	EN_STATUS_VMC	0: off 1: on

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Bit(s)	Name	Description
11	EN_STATUS_VMCH	0: off 1: on
10	EN_STATUS_VUSB33	0: off 1: on
9	EN_STATUS_VEMC33	0: off 1: on
8	EN_STATUS_VIO18	0: off 1: on
7	EN_STATUS_VIBR	0: off 1: on
6	EN_STATUS_TREF	0: off 1: on
5	EN_STATUS_VRTC	0: off 1: on
4	EN_STATUS_VPA	0: off 1: on
3	EN_STATUS_VPROC	0: off 1: on
2	EN_STATUS_VCORE	0: off 1: on
1	EN_STATUS_VS1	0: off 1: on

021A **THERMALSTATUS** **Thermal Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_THERMAL_STATUS															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	STRUP_THERMAL_STATUS	**Shutdown Thermal Status(clear by SW)** 0: no thermal 1: thermal occurred

021C **TOPSTATUS** **TOP Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														HOMEKEY_DEB	PWRKEY_DEB	
Type														RO	RO	
Reset														0	0	

Bit(s)	Name	Description

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Bit(s)	Name	Description
2	HOMEKEY_DEB	
1	PWRKEY_DEB	

021E **TDSEL_CON** **TDSEL_CON** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_E32CAL_TDSEL	RG_AUD_TDSEL	RG_SPI_TDSEL	RG_PMU_TDSEL
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_E32CAL_TDSEL	**TDSEL**
2	RG_AUD_TDSEL	**TDSEL**
1	RG_SPI_TDSEL	**TDSEL**
0	RG_PMU_TDSEL	**TDSEL**

0220 **RDSEL_CON** **RDSEL_CON** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_E32CAL_RDSEL	RG_AUD_RDSEL	RG_SPI_RDSEL	RG_PMU_RDSEL
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_E32CAL_RDSEL	**RDSEL**
2	RG_AUD_RDSEL	**RDSEL**
1	RG_SPI_RDSEL	**RDSEL**
0	RG_PMU_RDSEL	**RDSEL**

0222 **SMT_CON0** **SMT_CON0** **003C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_SMT_RTC_32K1V8_1	RG_SMT_RTC_32K1V8_0	RG_SMT_SRCLKEN_IN1	RG_SMT_SRCLKEN_IN0	RG_SMT_HOMEKEY	RG_SMT_WDTRSTB_IN
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	0	0

Bit(s)	Name	Description
5	RG_SMT_RTC_32K1V8_1	**SMT** 0: Disable

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Bit(s)	Name	Description
		1: Enable
4	RG_SMT_RTC_32K1V8_0	**SMT** 0: Disable 1: Enable
3	RG_SMT_SRCLKEN_IN1	**SMT** 0: Disable 1: Enable
2	RG_SMT_SRCLKEN_IN0	**SMT** 0: Disable 1: Enable
1	RG_SMT_HOMEKEY	**SMT** 0: Disable 1: Enable
0	RG_SMT_WDTRSTB_IN	**SMT** 0: Disable 1: Enable

0224 SMT_CON1 SMT_CON1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_SMT_SPI_MISO	RG_SMT_SPI_MOSI	RG_SMT_SPI_CSN	RG_SMT_SPI_CLK
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_SMT_SPI_MISO	**SMT** 0: Disable 1: Enable
2	RG_SMT_SPI_MOSI	**SMT** 0: Disable 1: Enable
1	RG_SMT_SPI_CSN	**SMT** 0: Disable 1: Enable
0	RG_SMT_SPI_CLK	**SMT** 0: Disable 1: Enable

0226 SMT_CON2 SMT_CON2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_SMT_XOSC_EN	RG_SMT_ENBB	RG_SMT_VOW_CLK_MISO	RG_SMT_ANC_DAT_MOSI	RG_SMT_AUD_DAT_MISO	RG_SMT_AUD_DAT_MOSI	RG_SMT_AUD_CLK
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

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Bit(s)	Name	Description
6	RG_SMT_XOSC_EN	**SMT** 0: Disable 1: Enable
5	RG_SMT_ENBB	**SMT** 0: Disable 1: Enable
4	RG_SMT_VOW_CLK_MISO	**SMT** 0: Disable 1: Enable
3	RG_SMT_ANC_DAT_MOSI	**SMT** 0: Disable 1: Enable
2	RG_SMT_AUD_DAT_MISO	**SMT** 0: Disable 1: Enable
1	RG_SMT_AUD_DAT_MOSI	**SMT** 0: Disable 1: Enable
0	RG_SMT_AUD_CLK	**SMT** 0: Disable 1: Enable

0228 **DRV_CON0** **DRV_CON0** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_RTC_32K1V8_1				RG_OCTL_RTC_32K1V8_0				RG_OCTL_SRCLKEN_IN1				RG_OCTL_SRCLKEN_IN0			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_RTC_32K1V8_1	**OC CTL**
11:8	RG_OCTL_RTC_32K1V8_0	**OC CTL**
7:4	RG_OCTL_SRCLKEN_IN1	**OC CTL**
3:0	RG_OCTL_SRCLKEN_IN0	**OC CTL**

022A **DRV_CON1** **DRV_CON1** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_SPI_MISO				RG_OCTL_SPI_MOSI				RG_OCTL_SPI_CSN				RG_OCTL_SPI_CLK			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_SPI_MISO	**OC CTL**
11:8	RG_OCTL_SPI_MOSI	**OC CTL**

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Bit(s)	Name	Description
7:4	RG_OCTL_SPI_CSN	**OC CTL**
3:0	RG_OCTL_SPI_CLK	**OC CTL**

022C **DRV_CON2** **DRV_CON2** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OCTL_ANC_DAT_MOSI**				**RG_OCTL_AUD_CLK**				**RG_OCTL_AUD_DAT_MISO**				**RG_OCTL_AUD_DAT_MOSI**			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_ANC_DAT_MOSI	**OC CTL**
11:8	RG_OCTL_AUD_CLK	**OC CTL**
7:4	RG_OCTL_AUD_DAT_MISO	**OC CTL**
3:0	RG_OCTL_AUD_DAT_MOSI	**OC CTL**

022E **DRV_CON3** **DRV_CON3** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OCTL_VOW_CLK_MISO**				**RG_OCTL_XOSC_EN**				**RG_OCTL_ENBB**				**RG_OCTL_HOMEKEY**			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_VOW_CLK_MISO	**OC CTL**
11:8	RG_OCTL_XOSC_EN	**OC CTL**
7:4	RG_OCTL_ENBB	**OC CTL**
3:0	RG_OCTL_HOMEKEY	**OC CTL**

0230 **TOP_STATUS** **TOP_STATUS** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**TOP_STATUS**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TOP_STATUS	

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0238 **CLK_BUCK_CON0** **CLK_BUCK control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CLK_VOWEN_MODE	CLK_BUCK_OSC_SEL_MODE		CLK_SRCVOLTEN_MODE	CLK_VOWEN_SW	CLK_BUCK_OSC_SEL_SW		CLK_SRCVOLTEN_SW
Type									RW	RW		RW	RW	RW		RW
Reset									0	0		0	0	0		0

Bit(s)	Name	Description
7	CLK_VOWEN_MODE	**VOWEN mode** 1'b0: HW mode 1'b1: SW mode
6	CLK_BUCK_OSC_SEL_MODE	**BUCK_OSC_SEL mode** 1'b0: HW mode 1'b1: SW mode
4	CLK_SRCVOLTEN_MODE	**SRCVOLTEN mode** 1'b0: HW mode 1'b1: SW mode
3	CLK_VOWEN_SW	**VOWEN SW mode value**
2	CLK_BUCK_OSC_SEL_SW	**BUCK_OSC_SEL SW mode value**
0	CLK_SRCVOLTEN_SW	**SRCVOLTEN SW mode value**

023A **CLK_BUCK_CON0_SET** **CLK_BUCK control register 0_SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_BUCK_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_BUCK_CON0_SET	**Set CLK_BUCK_CON0** 1'b0: no set 1'b1: set

023C **CLK_BUCK_CON0_CLR** **CLK_BUCK control register 0_CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_BUCK_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_BUCK_CON0_C	**Clear CLK_BUCK_CON0**

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Bit(s)	Name	Description
	LR	1'b0: no clear 1'b1: clear

0240 **CLK_BUCK_CON1_SET** **CLK_BUCK control register 1_SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_BUCK_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_BUCK_CON1_SET	**Set CLK_BUCK_CON1** 1'b0: no set 1'b1: set

0242 **CLK_BUCK_CON1_CLR** **CLK_BUCK control register 1_CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_BUCK_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_BUCK_CON1_CLR	**Clear CLK_BUCK_CON1** 1'b0: no clear 1'b1: clear

0244 **TOP_CLKSQ** **TOP_CLKSQ register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CLKSQ_EN_VA28				RG_CLKSQ_IN_SEL_VA18_SWCTRL	RG_CLKSQ_IN_SEL_VA18	RG_CLKSQ_EN_AUX_MD_MODE	RG_CLKSQ_EN_AUX_AP_MODE				RG_CLKSQ_EN_AUX_GPS	RG_CLKSQ_EN_AUX_MD	RG_CLKSQ_EN_AUX_AP	RG_CLKSQ_EN_FQR	RG_CLKSQ_EN_AUD
Type	RO				RW	RW	RW	RW				RW	RW	RW	RW	RW
Reset	0				0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15	DA_CLKSQ_EN_VA28	**Status of CLKSQ** 0: Disable 1: Enable
11	RG_CLKSQ_IN_SEL_VA18_SWCTRL	**CLKSQ_IN_SEL_VA18 sw control** 0: HW control 1: SW control
10	RG_CLKSQ_IN_SEL_	**CLKSQ_IN_SEL_VA18 sw enable**

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Bit(s)	Name	Description
	VA18	0: SW mode 1: HW mode: SRCLKEN_IN0
9	RG_CLKSQ_EN_AUX_MD_MODE	**Select CLKSQ_EN_AUX_MD mode** 0: SW mode 1: HW mode: SRCLKEN_IN0
8	RG_CLKSQ_EN_AUX_AP_MODE	**Select CLKSQ_EN_AUX_AP mode** 0: SW mode 1: HW mode: SRCLKEN_IN0
4	RG_CLKSQ_EN_AUX_GPS	**Enable CLKSQ for GPS** 0: Disable clock 1: Enable clock
3	RG_CLKSQ_EN_AUX_MD	**Enable CLKSQ for MD (SW mode)** 0: Disable clock 1: Enable clock
2	RG_CLKSQ_EN_AUX_AP	**Enable CLKSQ for AP (SW mode)** 0: Disable clock 1: Enable clock
1	RG_CLKSQ_EN_FQR	**Enable CLKSQ for FQMTR** 0: Disable clock 1: Enable clock
0	RG_CLKSQ_EN_AUD	**Enable CLKSQ for AUDIO** 0: Disable clock 1: Enable clock

0246 TOP_CLKSQ_SET TOP_CLKSQ register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_SET	**Set TOP_CLKSQ** 1'b0: no set 1'b1: set

0248 TOP_CLKSQ_CLR TOP_CLKSQ register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_CLR	**Clear TOP_CLKSQ** 1'b0: no clear 1'b1: clear

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024A **TOP_CLKSQ_RTC** **TOP_CLKSQ_RTC register** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_CLKSQ_EN_VDIG18**														**RG_CLKSQ_RTC_EN_HW_MODE**	**RG_CLKSQ_RTC_EN**
Type	RO														RW	RW
Reset	0														1	0

Bit(s)	Name	Description
15	DA_CLKSQ_EN_VDIG18	**Status of CLKSQ_RTC** 0: Disable 1: Enable
1	RG_CLKSQ_RTC_EN_HW_MODE	**The CLKSQ_RTC HW mode** If enable, CLKSQ_RTC will be from HW control If disable, CLKSQ_RTC will be from RG_CLKSQ_RTC_EN 0: SW mode 1: HW mode
0	RG_CLKSQ_RTC_EN	**Enable CLKSQ_RTC** 0: Disable clock 1: Enable clock

024C **TOP_CLKSQ_RTC_SET** **TOP_CLKSQ_RTC register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TOP_CLKSQ_RTC_SET**															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_RTC_SET	**Set TOP_CLKSQ_RTC** 1'b0: no set 1'b1: set

024E **TOP_CLKSQ_RTC_CLR** **TOP_CLKSQ_RTC register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TOP_CLKSQ_RTC_CLR**															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_RTC_CLR	**Clear TOP_CLKSQ_RTC** 1'b0: no clear 1'b1: clear

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0250 **TOP_CLK_TRIM** **TOP_CLK_TRIM register** **0C6C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DA_OSC_75K_TRIM												
Type				RO												
Reset				0	1	1	0	0								

Bit(s)	Name	Description
12:8	DA_OSC_75K_TRIM	**75KHz OSC trimming bit**

0256 **CLK_PDN_CON0** **CLK_PDN control register 0** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLK_RTC_2SEC_OFF_DET_PDN	CLK_RTC32K_1V8_1_O_PDN	CLK_RTC32K_1V8_0_O_PDN
Type														RW	RW	RW
Reset														0	1	0

Bit(s)	Name	Description
2	CLK_RTC_2SEC_OFF_DET_PDN	**_RTC_2SEC_OFF_DET power down** 0: Power on 1: Power down
1	CLK_RTC32K_1V8_1_O_PDN	**_RTC32K_1V8_1_O power down** 0: Power on 1: Power down
0	CLK_RTC32K_1V8_0_O_PDN	**_RTC32K_1V8_0_O power down** 0: Power on 1: Power down

0258 **CLK_PDN_CON0_SET** **CLK_PDN control register 0_SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_PDN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_PDN_CON0_SET	**Set CLK_PDN_CON0** 1'b0: no set 1'b1: set

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025A **CLK_PDN_CON0_CLR** **CLK_PDN control register 0_CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_PDN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_PDN_CON0_CLR	**Clear CLK_PDN_CON0** 1'b0: no clear 1'b1: clear

025C **CLK_PDN_CON1** **CLK_PDN control register 1** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLK_BUCK_ANA_CK_PDN		CLK_SMPS_CK_DIV_PDN	CLK_ZCD13M_CK_PDN
Type													RW		RW	RW
Reset													0		0	1

Bit(s)	Name	Description
3	CLK_BUCK_ANA_CK_PDN	**_BUCK_ANA_CK power down** 0: Power on 1: Power down
1	CLK_SMPS_CK_DIV_PDN	**_SMPS_CK_DIV power down** 0: Power on 1: Power down
0	CLK_ZCD13M_CK_PDN	**_ZCD13M_CK power down** 0: Power on 1: Power down

025E **CLK_PDN_CON1_SET** **CLK_PDN control register 1_SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_PDN_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_PDN_CON1_SET	**Set CLK_PDN_CON1** 1'b0: no set 1'b1: set

0260 **CLK_PDN_CO** **CLK_PDN control register 1_CLR** **0000**

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N1_CLR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_PDN_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_PDN_CON1_CLR	**Clear CLK_PDN_CON1** 1'b0: no clear 1'b1: clear

0262 CLK_SEL_CON0 CLK_SEL control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CLK_SRCLKEN_SRC_SEL		CLK_OSC_SEL_HW_SRC_SEL	
Type													RW		RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3:2	CLK_SRCLKEN_SRC_SEL	**srclken source seletcion** 2'b00: from srclken0 2'b01: from srclken1 2'b10: from srclken0 and srclken1 2'b11: Reserved
1:0	CLK_OSC_SEL_HW_SRC_SEL	**OSC_SEL source seletcion under hardware control** 2'b00: from buck controller 2'b01: from srclken 2'b10: Reserved 2'b11: Reserved

0264 CLK_SEL_CON0_SET CLK_SEL control register 0_SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_SEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_SEL_CON0_SET	**Set CLK_SEL_CON0** 1'b0: no set 1'b1: set

0266 CLK_SEL_CON0_CLR CLK_SEL control register 0_CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_SEL_CON0_CLR															

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Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_SEL_CON0_CLR	**Clear CLK_SEL_CON0** 1'b0: no clear 1'b1: clear

0268 **CLK_SEL_CON1** **CLK_SEL control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLK_75K_32K_SEL	CLK_AUXADC_CK_CKSEL	CLK_AUXADC_CK_CKSEL_HWEN
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	CLK_75K_32K_SEL	**RTC_32K1V8_CK clock selection** 1'b0: R_PMU75K_CK/2 1'b1: R_RTC32K_CK
1	CLK_AUXADC_CK_CKSEL	**_AUXADC_CK clock selection** 1'b0: R_SMPS_CK/n 1'b1: R_AUD26_CK/n
0	CLK_AUXADC_CK_CKSEL_HWEN	**AUXADC_CK clock selection control** 0: SW mode 1: HW mode

026A **CLK_SEL_CON1_SET** **CLK_SEL control register 1_SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_SEL_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_SEL_CON1_SET	**Set CLK_SEL_CON1** 1'b0: no set 1'b1: set

026C **CLK_SEL_CON1_CLR** **CLK_SEL control register 1_CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_SEL_CON1_CLR															

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Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_SEL_CON1_CLR	**Clear CLK_SEL_CON1** 1'b0: no clear 1'b1: clear

026E **CLK_CKPDN_CON0** **CLK_CKPDN control register 0** **FF6C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_DRV_ISINK3_CK_PDN	CLK_DRV_ISINK2_CK_PDN	CLK_DRV_ISINK1_CK_PDN	CLK_DRV_ISINK0_CK_PDN	CLK_AUXADC_CK_PDN	CLK_AUXADC_26M_CK_PDN	CLK_AUXADC_RNG_CK_PDN	CLK_AUXADC_SMPS_CK_PDN	CLK_AUXADC_1M_CK_PDN	CLK_AUDNCP_CK_PDN	CLK_AUD_CK_PDN	CLK_AUDIF_CK_PDN	CLK_ACCDET_CK_PDN	CLK_G_SMPS_TEST_CK_PDN	CLK_G_SMPS_AUD_CK_PDN	CLK_G_SMPS_PD_CK_PDN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	0	1	1	0	1	1	0	0

Bit(s)	Name	Description
15	CLK_DRV_ISINK3_CK_PDN	**[DRIVER] DRV_ISINK3_CK power down** 0: Power on 1: Power down
14	CLK_DRV_ISINK2_CK_PDN	**[DRIVER] DRV_ISINK2_CK power down** 0: Power on 1: Power down
13	CLK_DRV_ISINK1_CK_PDN	**[DRIVER] DRV_ISINK1_CK power down** 0: Power on 1: Power down
12	CLK_DRV_ISINK0_CK_PDN	**[DRIVER] DRV_ISINK0_CK power down** 0: Power on 1: Power down
11	CLK_AUXADC_CK_PDN	**[AUXADC] AUXADC_CK power down** 0: Power on 1: Power down
10	CLK_AUXADC_26M_CK_PDN	**[AUXADC] AUXADC_26M_CK power down** 0: Power on 1: Power down
9	CLK_AUXADC_RNG_CK_PDN	**[AUXADC] AUXADC_RNG_CK power down** 0: Power on 1: Power down
8	CLK_AUXADC_SMPS_CK_PDN	**[AUXADC] AUXADC_SMPS_CK power down** 0: Power on 1: Power down
7	CLK_AUXADC_1M_CK_PDN	**[AUXADC] AUXADC_1M_CK power down** 0: Power on 1: Power down
6	CLK_AUDNCP_CK_PDN	**[AUDNCP] AUDNCP_CK power down** 0: Power on 1: Power down
5	CLK_AUD_CK_PDN	**[AUDIO] AUD_CK power down**

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Bit(s)	Name	Description
		0: Power on 1: Power down
4	CLK_AUDIF_CK_PDN	**[AUDIO] AUDIF_CK power down** 0: Power on 1: Power down
3	CLK_ACCDET_CK_PDN	**[ACCDET] ACCDET_CK power down** 0: Power on 1: Power down
2	CLK_G_SMPS_TEST_CK_PDN	**[TOP] G_SMPS_TEST_CK power down** 0: Power on 1: Power down
1	CLK_G_SMPS_AUD_CK_PDN	**[TOP] G_SMPS_AUD_CK power down** 0: Power on 1: Power down
0	CLK_G_SMPS_PD_CK_PDN	**[TOP] G_SMPS_PD_CK power down** 0: Power on 1: Power down

0270 **CLK_CKPDN_CON0_SET** **CLK_CKPDN SET control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_CON0_SET	**SET CLK_CKPDN_CON0** 1'b0: No set 1'b1: Set

0272 **CLK_CKPDN_CON0_CLR** **CLK_CKPDN CLR control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_CON0_CLR	**Clear CLK_CKPDN_CON0** 1'b0: No clear 1'b1: Clear

0274 **CLK_CKPDN_CON1** **CLK_CKPDN control register 1** **180A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_	CLK_

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	STB_1M_CK_PDN	INTRP_PRE_OC_CK_PDN	INTRP_CK_PDN	FQMTR_32K_CK_PDN	FQMTR_CK_PDN	BUCK_VS1_9M_CK_PDN	BUCK_VPA_9M_CK_PDN	BUCK_VCORE2_9M_CK_PDN	BUCK_VCORE_9M_CK_PDN	BUCK_VPROC_9M_CK_PDN	PWMOC_6M_CK_PDN	BUCK_9M_CK_PDN	BUCK_32K_CK_PDN	BUCK_1M_CK_PDN	DRV_32K_CK_PDN	DRV_CHRIND_CK_PDN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	1	0	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
15	CLK_STB_1M_CK_PDN	**[LDO] STB_1M_CK power down** 0: Power on 1: Power down
14	CLK_INTRP_PRE_OC_CK_PDN	**[INTCTL] INTRP_PRE_OC_CK power down** 0: Power on 1: Power down
13	CLK_INTRP_CK_PDN	**[INTCTL] INTRP_CK power down** 0: Power on 1: Power down
12	CLK_FQMTR_32K_CK_PDN	**[FQMTR] FQMTR_32K_CK power down** 0: Power on 1: Power down
11	CLK_FQMTR_CK_PDN	**[FQMTR] FQMTR_CK power down** 0: Power on 1: Power down
10	CLK_BUCK_VS1_9M_CK_PDN	**[BUCK] BUCK_VS1_9M_CK power down** 0: Power on 1: Power down
9	CLK_BUCK_VPA_9M_CK_PDN	**[BUCK] BUCK_VPA_9M_CK power down** 0: Power on 1: Power down
8	CLK_BUCK_VCORE2_9M_CK_PDN	**[BUCK] BUCK_VCORE2_9M_CK power down** 0: Power on 1: Power down
7	CLK_BUCK_VCORE_9M_CK_PDN	**[BUCK] BUCK_VCORE_9M_CK power down** 0: Power on 1: Power down
6	CLK_BUCK_VPROC_9M_CK_PDN	**[BUCK] BUCK_VPROC_9M_CK power down** 0: Power on 1: Power down
5	CLK_PWMOC_6M_CK_PDN	**[BUCK] PWMOC_6M_CK power down** 0: Power on 1: Power down
4	CLK_BUCK_9M_CK_PDN	**[BUCK] BUCK_9M_CK power down** 0: Power on 1: Power down
3	CLK_BUCK_32K_CK_PDN	**[BUCK] BUCK_32K_CK power down** 0: Power on 1: Power down
2	CLK_BUCK_1M_CK_PDN	**[BUCK] BUCK_1M_CK power down** 0: Power on 1: Power down
1	CLK_DRV_32K_CK_PDN	**[DRIVER] DRV_32K_CK power down** 0: Power on 1: Power down

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Bit(s)	Name	Description
0	CLK_DRV_CHRIND_CK_PDN	**[DRIVER] DRV_CHRIND_CK power down** 0: Power on 1: Power down

0276 **CLK_CKPDN_CON1_SET** **CLK_CKPDN SET control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_CON1_SET	**SET CLK_CKPDN_CON1** 1'b0: No set 1'b1: Set

0278 **CLK_CKPDN_CON1_CLR** **CLK_CKPDN CLR control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_CON1_CLR	**Clear CLK_CKPDN_CON1** 1'b0: No clear 1'b1: Clear

027A **CLK_CKPDN_CON2** **CLK_CKPDN control register 2** **0904**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_STRUP_32K_CK_PDN	CLK_STRUP_75K_CK_PDN	CLK_EFUSE_CK_PDN	CLK_TRIM_75K_CK_PDN	CLK_FGADC_FT_CK_PDN	CLK_FGADC_DIG_CK_PDN	CLK_FGADC_ANA_CK_PDN	CLK_EOSC_CALI_TEST_CK_PDN	CLK_RTC_EOSC32_CK_PDN	CLK_RTCDET_CK_PDN	CLK_RTC_75K_CK_PDN	CLK_RTC_MCLK_PDN	CLK_RTC_32K_CK_PDN	CLK_RTC_26M_CK_PDN	CLK_LDO_VSRAM_PROC_9M_CK_PDN	CLK_LDO_CALI_75K_CK_PDN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15	CLK_STRUP_32K_CK_PDN	**[STRUP] STRUP_32K_CK power down** 0: Power on 1: Power down
14	CLK_STRUP_75K_CK	**[STRUP] STRUP_75K_CK power down**

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Bit(s)	Name	Description
	_PDN	0: Power on 1: Power down
13	CLK_EFUSE_CK_PDN	**[EFUSE] EFUSE_CK power down** 0: Power on 1: Power down
12	CLK_TRIM_75K_CK_PDN	**[TRIM_75K] TRIM_75K_CK power down** 0: Power on 1: Power down
11	CLK_FGADC_FT_CK_PDN	**[FGADC] FGADC_FT_CK power down** 0: Power on 1: Power down
10	CLK_FGADC_DIG_CK_PDN	**[FGADC] FGADC_DIG_CK power down** 0: Power on 1: Power down
9	CLK_FGADC_ANA_CK_PDN	**[FGADC] FGADC_ANA_CK power down** 0: Power on 1: Power down
8	CLK_EOSC_CALI_TEST_CK_PDN	**[RTC] EOSC_CALI_TEST_CK power down** 0: Power on 1: Power down
7	CLK_RTC_EOSC32_CK_PDN	**[RTC] RTC_EOSC32_CK power down** 0: Power on 1: Power down
6	CLK_RTCDET_CK_PDN	**[RTC] RTCDET_CK power down** 0: Power on 1: Power down
5	CLK_RTC_75K_CK_PDN	**[RTC] RTC_75K_CK power down** 0: Power on 1: Power down
4	CLK_RTC_MCLK_PDN	**[RTC] RTC_MCLK power down** 0: Power on 1: Power down
3	CLK_RTC_32K_CK_PDN	**[RTC] RTC_32K_CK power down** 0: Power on 1: Power down
2	CLK_RTC_26M_CK_PDN	**[RTC] RTC_26M_CK power down** 0: Power on 1: Power down
1	CLK_LDO_VSRAM_PROC_9M_CK_PDN	**[LDO] LDO_VSRAM_PROC_9M_CK power down** 0: Power on 1: Power down
0	CLK_LDO_CALI_75K_CK_PDN	**[LDO] LDO_CALI_75K_CK power down** 0: Power on 1: Power down

027C **CLK_CKPDN_CON2_SET** **CLK_CKPDN SET control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_CON2_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	CLK_CKPDN_CON2_SET	**SET CLK_CKPDN_CON2** 1'b0: No set 1'b1: Set

027E **CLK_CKPDN_CON2_CLR** CLK_CKPDN CLR control register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_CON2_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_CON2_CLR	**Clear CLK_CKPDN_CON2** 1'b0: No clear 1'b1: Clear

0280 **CLK_CKPDN_CON3** CLK_CKPDN control register 3 00CA

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_RSV_PDN								CLK_SPK_PWM_CK_PDN	CLK_SPK_CK_PDN	CLK_TYPE_C_CSR_CK_PDN	CLK_TYPE_C_CC_CK_PDN	CLK_BGR_TEST_CK_PDN	CLK_SPI_CK_PDN	CLK_PCHR_TEST_CK_PDN	CLK_PCHR_32K_CK_PDN
Type	RW								RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	0	1	0

Bit(s)	Name	Description
15:8	CLK_RSV_PDN	**[RSV] RSV power down** 0: Power on 1: Power down
7	CLK_SPK_PWM_CK_PDN	**[SPK] SPK_PWM_CK power down** 0: Power on 1: Power down
6	CLK_SPK_CK_PDN	**[SPK] SPK_CK power down** 0: Power on 1: Power down
5	CLK_TYPE_C_CSR_CK_PDN	**[TYPE_C] TYPE_C_CSR_CK power down** 0: Power on 1: Power down
4	CLK_TYPE_C_CC_CK_PDN	**[TYPE_C] TYPE_C_CC_CK power down** 0: Power on 1: Power down
3	CLK_BGR_TEST_CK_PDN	**[TOP] BGR_TEST_CK power down** 0: Power on 1: Power down
2	CLK_SPI_CK_PDN	**[SPI] SPI_CK power down**

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Bit(s)	Name	Description
		0: Power on 1: Power down
1	CLK_PCHR_TEST_CK_PDN	**[PCHR] PCHR_TEST_CK power down** 0: Power on 1: Power down
0	CLK_PCHR_32K_CK_PDN	**[PCHR] PCHR_32K_CK power down** 0: Power on 1: Power down

0282 CLK_CKPDN_CON3_SET CLK_CKPDN SET control register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_CON3_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_CON3_SET	**SET CLK_CKPDN_CON3** 1'b0: No set 1'b1: Set

0284 CLK_CKPDN_CON3_CLR CLK_CKPDN CLR control register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_CON3_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_CON3_CLR	**Clear CLK_CKPDN_CON3** 1'b0: No clear 1'b1: Clear

0286 CLK_CKPDN_HWEN_CON0 CLK_CKPDN_HWEN control register 0 3FF7

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_RSV_PDN_HWEN		CLK_RTC_26M_CK_PDN_HWEN	CLK_LDO_VSRAM_PROC_9M_CK_PDN_HWEN	CLK_STB_1M_CK_PDN_HWEN	CLK_BUCK_VS1_9M_CK_PDN_HWEN	CLK_BUCK_VPA_9M_CK_PDN_HWEN	CLK_BUCK_VCORE2_9M_CK_PDN_HWEN	CLK_BUCK_VCORE_9M_CK_PDN_HWEN	CLK_BUCK_VPROC_9M_CK_PDN_HWEN	CLK_BUCK_1M_CK_PDN_HWEN	CLK_AUXADC_CK_PDN_HWEN	CLK_AUXADC_26M_CK_PDN_HWEN	CLK_AUXADC_SMPS_CK_PDN_HWEN	CLK_G_SMPS_AUD_CK_PDN_HWEN	CLK_G_SMPS_PD_CK_PDN_HWEN
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1

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Bit(s)	Name	Description
15:14	CLK_RSV_PDN_HWEN	**[RSV] RSV's power down control mode** 0: SW mode 1: HW mode
13	CLK_RTC_26M_CK_PDN_HWEN	**[RTC] RTC_26M_CK's power down control mode** 0: SW mode 1: HW mode
12	CLK_LDO_VSRAM_PROC_9M_CK_PDN_HWEN	**[LDO] LDO_VSRAM_PROC_9M_CK's power down control mode** 0: SW mode 1: HW mode
11	CLK_STB_1M_CK_PDN_HWEN	**[LDO] STB_1M_CK's power down control mode** 0: SW mode 1: HW mode
10	CLK_BUCK_VS1_9M_CK_PDN_HWEN	**[BUCK] BUCK_VS1_9M_CK's power down control mode** 0: SW mode 1: HW mode
9	CLK_BUCK_VPA_9M_CK_PDN_HWEN	**[BUCK] BUCK_VPA_9M_CK's power down control mode** 0: SW mode 1: HW mode
8	CLK_BUCK_VCORE2_9M_CK_PDN_HWEN	**[BUCK] BUCK_VCORE2_9M_CK's power down control mode** 0: SW mode 1: HW mode
7	CLK_BUCK_VCORE_9M_CK_PDN_HWEN	**[BUCK] BUCK_VCORE_9M_CK's power down control mode** 0: SW mode 1: HW mode
6	CLK_BUCK_VPROC_9M_CK_PDN_HWEN	**[BUCK] BUCK_VPROC_9M_CK's power down control mode** 0: SW mode 1: HW mode
5	CLK_BUCK_1M_CK_PDN_HWEN	**[BUCK] BUCK_1M_CK's power down control mode** 0: SW mode 1: HW mode
4	CLK_AUXADC_CK_PDN_HWEN	**[AUXADC] AUXADC_CK's power down control mode** 0: SW mode 1: HW mode
3	CLK_AUXADC_26M_CK_PDN_HWEN	**[AUXADC] AUXADC_26M_CK's power down control mode** 0: SW mode 1: HW mode
2	CLK_AUXADC_SMPS_CK_PDN_HWEN	**[AUXADC] AUXADC_SMPS_CK's power down control mode** 0: SW mode 1: HW mode
1	CLK_G_SMPS_AUD_CK_PDN_HWEN	**[TOP] G_SMPS_AUD_CK's power down control mode** 0: SW mode 1: HW mode
0	CLK_G_SMPS_PD_CK_PDN_HWEN	**[TOP] G_SMPS_PD_CK's power down control mode** 0: SW mode 1: HW mode

0288 **CLK_CKPDN_HWEN_CON0_SET** **CLK_CKPDN_HWEN SET control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	CLK_CKPDN_HWEN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_HWEN_CON0_SET	**SET CLK_CKPDN_HWEN_CON0** 1'b0: No set 1'b1: Set

028A CLK_CKPDN_HWEN_CON0_CLR CLK_CKPDN_HWEN CLR control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKPDN_HWEN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKPDN_HWEN_CON0_CLR	**Clear CLK_CKPDN_HWEN_CON0** 1'b0: No clear 1'b1: Clear

028C CLK_CKSEL_CON0 CLK_CKSEL control register 0 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CLK_EFUSE_CK_PDN_HWEN								
Type								RW								
Reset								1								

Bit(s)	Name	Description
8	CLK_EFUSE_CK_PDN_HWEN	**[EFUSE] EFUSE_CK's power down control mode** 0: SW mode 1: HW mode

028E CLK_CKSEL_CON0_SET CLK_CKSEL SET control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKSEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKSEL_CON0_	**SET CLK_CKSEL_CON0**

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Bit(s)	Name	Description
	SET	1'b0: No set 1'b1: Set

0290 **CLK_CKSEL_CON0_CLR** **CLK_CKSEL CLR control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKSEL_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKSEL_CON0_CLR	**Clear CLK_CKSEL_CON0** 1'b0: No clear 1'b1: Clear

0292 **CLK_CKDIVSEL_CON0** **CLK_CKDIVSEL control register 0** **0015**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CLK_SPK_PWM_CK_DIVSEL		CLK_SPK_CK_DIVSEL		CLK_REG_CK_DIVSEL				CLK_BUCK_9M_CK_DIVSEL	CLK_AUXADC_26M_CK_DIVSEL		CLK_AUXADC_SMPS_CK_DIVSEL	
Type				RW		RW		RW				RW	RW		RW	
Reset				0	0	0	0	0	0			1	0	1	0	1

Bit(s)	Name	Description
12:11	CLK_SPK_PWM_CK_DIVSEL	**[SPK] SPK_PWM_CK's clock divider selection** 2'b00: DIV1 2'b01: DIV16 2'b10: DIV32 2'b11: DIV64
10:9	CLK_SPK_CK_DIVSEL	**[SPK] SPK_CK's clock divider selection** 2'b00: DIV1 2'b01: DIV2 2'b10: DIV4 2'b11: DIV8
8:7	CLK_REG_CK_DIVSEL	**[REG] REG_CK's clock divider selection** 2'b00: DIV1 2'b01: DIV2 2'b10: DIV4 2'b11: DIV8
4	CLK_BUCK_9M_CK_DIVSEL	**[BUCK] BUCK_9M_CK's clock divider selection** 1'b0: DIV1 1'b1: DIV2
3:2	CLK_AUXADC_26M_CK_DIVSEL	**[AUXADC] AUXADC_26M_CK's clock divider selection** 2'b00: DIV26 2'b01: DIV13 2'b1x: DIV8

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Bit(s)	Name	Description
1:0	CLK_AUXADC_SMPS_CK_DIVSEL	**[AUXADC] AUXADC_SMPS_CK's clock divider selection** 2'b00: DIV18 2'b01: DIV9 2'b10: DIV6 2'b11: DIV4

0294 **CLK_CKDIVSEL_CON0_SET** **CLK_CKDIVSEL SET control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKDIVSEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKDIVSEL_CON0_SET	**SET CLK_CKDIVSEL_CON0** 1'b0: No set 1'b1: Set

0296 **CLK_CKDIVSEL_CON0_CLR** **CLK_CKDIVSEL CLR control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CLK_CKDIVSEL_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CLK_CKDIVSEL_CON0_CLR	**Clear CLK_CKDIVSEL_CON0** 1'b0: No clear 1'b1: Clear

02AE **TOP_RST_STATUS** **TOP_RST_STATUS register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														UVLO_RSTB_STATUS	DDLO_RSTB_STATUS	
Type														RW	RW	
Reset														0	0	

Bit(s)	Name	Description
2	UVLO_RSTB_STATUS	**Status of UVLO_RSTB**
1	DDLO_RSTB_STATUS	**Status of DDLO_RSTB**

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02E0 SPK_CON0 Speaker Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_SPK_GAINL			SPK_OUT_STAGE_SEL	SPK_THER_SHDN_L_EN	SPK_OC_SHDN_DL					SPK_TRIM_EN_L	SPKMODE_L		SPK_EN_L
Type			RW			RW	RW	RW					RW	RW		RW
Reset			0	0		0	0	0					0	0		0

Bit(s)	Name	Description
13:12	RG_SPK_GAINL	**Controls speaker L-ch volume** 2'b00: Mute 2'b01: -6dB 2'b10: -3dB 2'b11: 0dB
10	SPK_OUT_STAGE_SEL	**Selects OUTSTAGE after triming enabled** 1'b0: Disable 1'b1: Enable
9	SPK_THER_SHDN_L_EN	**Enables speaker L-ch thermal shut-down** 1'b0: Disable 1'b1: Enable
8	SPK_OC_SHDN_DL	**Class D mode L-ch OC event shut-down** 1'b0: Normal 1'b1: Shut down (turn off SPK output stage)
3	SPK_TRIM_EN_L	**Enables class D mode L-ch trimming** 1'b0: Disable 1'b1: Enable
2	SPKMODE_L	**Selects speaker L-ch driver mode** 1'b0: Class D mode 1'b1: Class AB mode
0	SPK_EN_L	**Enables speaker amp. L-ch** 1'b0: Disable 1'b1: Enable

02E2 SPK_CON1 Speaker Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPK_TRIM_DONE_L	SPK_OFFSET_L_MODE	SPK_LEAD_L_SW	SPK_OFFSET_L_SW					SPK_OFFSET_L_OV							
Type	RO	RW	RW	RW					RO							
Reset	0	0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
15	SPK_TRIM_DONE_L	**Class D mode L-ch trimming done** 1'b0: Not yet 1'b1: Done
14	SPK_OFFSET_L_MODE	**Selects SPK_OFFSET_L mode** 1'b0: Calibarion

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Bit(s)	Name	Description
		1'b1: Software register mode
13	SPK_LEAD_L_SW	**Class D L-ch PWM polarity flag**
12:8	SPK_OFFSET_L_SW	**Speaker amplifier left channel offset triming bit** 5'b00000: 0mV 5'b00001: 0.6mV 5'b00010: 1.2mV xxx: xxxV (omit) 5'b11111: 18.6mV
7	SPK_OFFSET_L_OV	**SPK_OFFSET_L overflow**

02E4 SPK_CON2 Speaker Control Register 2 0014

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**RG_SPK_OC_EN_L**	**RG_SPKAB_OC_EN_L**	**RG_SPK_TEST_EN_L**	**RG_SPK_DRC_EN_L**	**RG_SPKRCV_EN_L**	**RG_SPKAB_OBIAS_L**		**RG_SPK_SLEW_L**		**RG_SPK_FORCE_EN_L**	**RG_SPK_INTG_RST_L**
Type						RW	RW	RW	RW	RW	RW		RW		RW	RW
Reset						0	0	0	0	0	0	1	0	1	0	0

Bit(s)	Name	Description
10	RG_SPK_OC_EN_L	**Enables class D L-ch over-current protection** 1'b0: Disable 1'b1: Enable
9	RG_SPKAB_OC_EN_L	**Enables class AB mode L-ch Over-current protection**
8	RG_SPK_TEST_EN_L	**Enables test input into SPK stage** (Not used)
7	RG_SPK_DRC_EN_L	**Reserved** (Not used)
6	RG_SPKRCV_EN_L	**Reserved** 1'b0: Disable 1'b1: Enable
5:4	RG_SPKAB_OBIAS_L	**Controsl L-ch classAB SPK bias** 00: 2I 11: 8I step=2I
3:2	RG_SPK_SLEW_L	**Controls class D L-ch slew rate** 00: 3/4 (default)10.8n /8.3n (rise/fall) 01: 4/4 8.8n /6.3n 10: 1/4 16.4n /15n 11: 2/4 3.8n/12.6n
1	RG_SPK_FORCE_EN_L	**Forces L-ch class D output state** 1'b0: Disable 1'b1: Enable
0	RG_SPK_INTG_RST_L	**Controls speaker L-ch integrator reset** 1'b0: No reset 1'b1: Reset on

02EC SPK_CON6 Speaker Control Register 6 0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPK_AB_OC_L_DEG	SPK_D_OC_L_DEG			SPK_OC_THD		SPK_OC_WND				SPK_TRIM_THD			SPK_TRIM_WND		
Type	RO	RO			RW		RW				RW			RW		
Reset	0	0			0	0	0	0			0	0		0	0	0

Bit(s)	Name	Description
15	SPK_AB_OC_L_DEG	**Class AB L-ch OC flag with deglitch**
14	SPK_D_OC_L_DEG	**Class D L-ch OC flag with deglitch**
11:10	SPK_OC_THD	**Threshold setting in the decision window for SPK over current status** 2'b00: 4/8 2'b01: 3/8 2'b10: 2/8 2'b11: 1/8
9:8	SPK_OC_WND	**Decision window setting for SPK over current status** 2'b00: 16us 2'b01: 32us 2'b10: 64us 2'b11: 128us
5:4	SPK_TRIM_THD	**Threshold setting in the decision window for SPK offset status** 2'b00: 4/8 2'b01: 3/8 2'b10: 2/8 2'b11: 1/8
2:0	SPK_TRIM_WND	**Decision window setting for SPK offset status** 3'b000: 16us 3'b001: 32us 3'b010: 64us 3'b011: 128us 3'b100: 256us 3'b101: 512us 3'b110: 1024us 3'b111: 2048us

02EE **SPK_CON7** **Speaker Control Register 7** **4531**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SPK_TRIM_DIV			SPK_TD3				SPK_TD2				SPK_TD1			
Type		RW			RW				RW				RW			
Reset		1	0	0	0	1	0	1	0	0	1	1	0	0	0	1

Bit(s)	Name	Description
14:12	SPK_TRIM_DIV	**Divider of AD_NI_SPK_CK_PWM for trimming counter clock** 3'b000: 8 3'b001: 16 3'b010: 32 3'b011: 64 3'b100: 128 3'b101: 256 3'b110: 512 3'b111: 1024
11:8	SPK_TD3	**Time delay3 for TRIM_EN** 4'd0: 0ms

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Bit(s)	Name	Description
		4'd1: 1ms 4'd2: 2ms 4'dN: nms 4'd15: 15ms
7:4	SPK_TD2	**Time delay2 for OUTSTG_EN** 4'd0: 0ms 4'd1: 1ms 4'd2: 2ms 4'dN: nms 4'd15: 15ms
3:0	SPK_TD1	**Time delay1 for VCM_FAST** 4'd0: 0ms 4'd1: 1ms 4'd2: 2ms 4'dN: nms 4'd15: 15ms

02F0 SPK_CON8 Speaker Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**RG_SPK_OCTH_D**	**RG_SPKAB_OVDRV**	**RG_SPK_FBRC_EN**	**RG_SPK_VCM_IBSEL**	**RG_SPK_VCM_SEL**	**RG_SPK_EN_VIEW_CLK**	**RG_SPK_EN_VIEW_VCM**	**RG_SPK_CCODE**				**RG_SPK_IBIAS_SEL**		**RG_BTL_SET**	
Type		RW	RW	RW	RW	RW	RW	RW	RW				RW		RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_SPK_OCTH_D	**Speaker OC threshold level for D-mode** 1'b0: Low (0.9A) 1'b1: High (1.5A)
13	RG_SPKAB_OVDRV	**Output stage shoot-through current prevention in over-drive condition of class AB mode** 1'b0: Disable 1'b1: Enable
12	RG_SPK_FBRC_EN	**Feedback grounded capacitor connection in class D state** 1'b0: Disable 1'b1: Enable
11	RG_SPK_VCM_IBSEL	**Selects speaker on-chip filter bias current level** 1'b0: Normal bias (low BW) 1'b1: Doubled bias (high BW)
10	RG_SPK_VCM_SEL	**Selects speaker VCM source** 1'b0: 0.5*AVDD43 1'b1: IR, I from BG
9	RG_SPK_EN_VIEW_CLK	**Enables mointor class D PWM CLK**
8	RG_SPK_EN_VIEW_VCM	**Enables mointor speaker VCM reference voltage**
7:4	RG_SPK_CCODE	**Class D modulation frequency control code** x000: 288k x001: 418.8k x010: 541k x011: 656k

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Bit(s)	Name	Description
		x100: 766k x101: 966k x110: 1.148M x111: 1.646M
3:2	RG_SPK_IBIAS_SEL	**Controls internal bias current generator** 2'b00: Default 2'b01: -20% 2'b10: +20% 2'b11: +10%
1:0	RG_BTL_SET	**Sets up class D BTL output when RG_FORCE_EN=1** <1> 1: SPK+ NMOS on; 0: SPK+ PMOS on <0> 1: SPK- NMOS on; 0: SPK- PMOS on

02F2 **SPK_CON9** **Speaker Control Register 9** **2000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPK_TEST_MODE1	SPK_TEST_MODE0	SPK_VCM_FAST_EN	SPK_RSV0	RG_SPKPGA_GAINL											
Type	RW	RW	RW	RW	RW											
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
15	SPK_TEST_MODE1	**SPK testmode 1**
14	SPK_TEST_MODE0	**SPK testmode 0**
13	SPK_VCM_FAST_EN	**Enables QI_SPK_VCM_FAST in hardware mode**
12	SPK_RSV0	
11:8	RG_SPKPGA_GAINL	**Controls speaker L PGA gain** 4'b0000: Mute 4'b0001: 0dB 4'b0010: 4dB 4'b0011: 5dB 4'b0100: 6dB 4'b0101: 7dB 4'b0110: 8dB 4'b0111: 9dB 4'b1000: 10dB 4'b1001: 11dB 4'b1010: 12dB 4'b1011: 13dB 4'b1100: 14dB 4'b1101: 15dB 4'b1110: 16dB 4'b1111: 17dB

02F4 **SPK_CON10** **Speaker Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SPK_TD_DONE				SPK_TD_WAIT		
Type										RW				RW		
Reset										0	0	0		0	0	0

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Bit(s)	Name	Description
6:4	SPK_TD_DONE	**Done time** 3'b000: 10us 3'b001: 50us 3'b010: 100us 3'b011: 300us 3'b100: 500us 3'b101: 1000us 3'b110: 1500us 3'b111: 2000us
2:0	SPK_TD_WAIT	**Wait time** 3'b000: 10us 3'b001: 50us 3'b010: 100us 3'b011: 300us 3'b100: 500us 3'b101: 1000us 3'b110: 1500us 3'b111: 2000us

02F6 SPK_CON11 Speaker Control Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPK_TRIM_STOP_L_SW		SPK_TRIM_EN_L_SW		SPK_OUTSTG_EN_L_SW		SPK_EN_L_SW		SPK_DEPOP_EN_L_SW		SPKMODE_L_SW		SPK_RST_L_SW		SPK_VCM_FAST_SW	SPK_EN_MODE
Type	RW		RW		RW		RW		RW		RW		RW		RW	RW
Reset	0		0		0		0		0		0		0		0	0

Bit(s)	Name	Description
15	SPK_TRIM_STOP_L_SW	**Class D mode offset trimming stop flag for L-ch**
13	SPK_TRIM_EN_L_SW	**Class D mode L-ch offset trimming start flag**
11	SPK_OUTSTG_EN_L_SW	**Spekaer left channel output stage enable control**
9	SPK_EN_L_SW	**Enables speaker amp. L-ch** 1'b0: Disable 1'b1: Enable
7	SPK_DEPOP_EN_L_SW	**Class D L-ch mode depop enabled flag**
5	SPKMODE_L_SW	**Selects speaker L-ch driver mode** 1'b0: Class D mode 1'b1: Class AB mode
3	SPK_RST_L_SW	**Resets class D L-ch** 1'b0: Normal 1'b1: Reset
1	SPK_VCM_FAST_SW	**Speeds up speaker VCM settling when enabled** 1'b0: Normal 1'b1: Fast charging
0	SPK_EN_MODE	**Selects speaker enable sequnece** 1'b0: HW 1'b1: SW (register mode)

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02F8 SPK_CON12 Speaker Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_ISENSE_EN	RG_SPK_ISENSE_PDRESET	RG_SPK_ISENSE_GAINSEL			RG_SPK_ISENSE_REFSEL			RG_SPK_ISENSE_TEST_EN							
Type	RW	RW	RW			RW			RW							
Reset	0	0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
15	RG_SPK_ISENSE_EN	**Enables class AB current sensing circuit** 1'b0: Disable 1'b1: Enable
14	RG_SPK_ISENSE_PDRESET	**Resets class AB current sensing peak detection** 1'b0: Disable 1'b1: Enable
13:11	RG_SPK_ISENSE_GAINSEL	**Selects class AB current sensing circuit gain** 3'b000: 0dB 3'b001: 6dB 3'b010: 12dB 3'b011: 18dB 3'b100: 24dB 3'b101: 30dB 3'b110~3'b111: Reserved
10:8	RG_SPK_ISENSE_REFSEL	**selects class AB current sensing circuit reference** 3'b000: AVSS43_SPK 3'b001: NMOS gate voltage @40uA 3'b010: NMOS gate voltage @80uA 3'b011: NMOS gate voltage @120uA 3'b100: NMOS gate voltage @160uA 3'b101: NMOS gate voltage @200uA 3'b110: NMOS gate voltage @240uA 3'b111: NMOS gate voltage @280uA
7	RG_SPK_ISENSE_TEST_EN	**(Not used)** 1'b0: Disable 1'b1: Enable

02FA SPK_CON13 Speaker Control Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_RSV0								RG_SPK_RSV1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_SPK_RSV0	**[15:14]: Not used** [13]: Enable Class-AB CLP [12:11]: Additional control on offset trimming circuit 2'b00: Normal operation (triangle modulation waveform) 2'b11: Trimming operation (sawtooth modulation waveform) [10]: RG_TRIM_INV

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Bit(s)	Name	Description
		1'b1: Inverting phase 1'b0: Default phase [9]: Enable Class-AB DFC (EN_AB_DFC) [8]: Enable PGA DLCK (EN_PGA_DLCK)
7:0	RG_SPK_RSV1	**(Not used)**

02FC **SPK_CON14** **Speaker Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_RSV2								RG_SPK_ABD_CURSEN_SEL	RG_SPK_ABD_VOLSEN_EN	RG_SPK_ABD_VOLSEN_GAIN					
Type	RW								RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15:8	RG_SPK_RSV2	**(Not used)**
7	RG_SPK_ABD_CURSEN_SEL	**(Not used)**
6	RG_SPK_ABD_VOLSEN_EN	**Controls class ABD voltage sensing** 1'b0: Disable 1'b1: Enable
5:4	RG_SPK_ABD_VOLSEN_GAIN	**Controls class ABD voltage sensing gain** 2'b00: -6dB 2'bx1: -18dB 2'b10: -12dB

02FE **SPK_CON15** **Speaker Control Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_TRIM1								RG_SPK_TRIM2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_SPK_TRIM1	**(Not used)**
7:0	RG_SPK_TRIM2	**(Not used)**

0300 **SPK_CON16** **Speaker Control Register 16** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_AB_CURSEN_EN	RG_SPK_AB_CURSEN_GAIN		RG_SPK_AB_CURSEN_RSETSEL					RG_SPK_D_CURSEN_EN	RG_SPK_D_CURSEN_GAIN		RG_SPK_D_CURSEN_RSETSEL				
Type	RW	RW		RW					RW	RW		RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	RG_SPK_AB_CURSEN_EN	**Controls class AB current sensing** 1'b0: Disable 1'b1: Enable
14:13	RG_SPK_AB_CURSEN_GAIN	**Controls class AB current sensing grain** 2'b00: -6dB 2'bx1: -18dB 2'b10: -12dB
12:8	RG_SPK_AB_CURSEN_RSETSEL	**(Not used)**
7	RG_SPK_D_CURSEN_EN	**(Not used)**
6:5	RG_SPK_D_CURSEN_GAIN	**(Not used)**
4:0	RG_SPK_D_CURSEN_RSETSEL	**(Not used)**

0302 SPK_ANA_CON0 SPK Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SPKPGA_GAIN														
Type		RW														
Reset		0	0	0	0											

Bit(s)	Name	Description
14:11	RG_SPKPGA_GAIN	**Controls speaker PGA gain** 0000: Mute 0001: 0dB 0010: 4dB 0011: 5dB 0100: 6dB 0101: 7dB 0110: 8dB 0111: 9dB 1000: 10dB 1001: 11dB 1010: 12dB 1011: 13dB 1100: 14dB 1101: 15dB 1110: 16dB 1111: 17dB

0304 SPK_ANA_CON1 SPK Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_ISENSE_PD_RESET				RG_SPK_RSV							

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type					RW				RW							
Reset					0				0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_ISENSE_PD_RESET	**Resets class AB current sensing peak detector** 0: Disable 1: Enable
7:0	RG_SPK_RSV	**Reserved**

0306 **SPK_ANA_CON3** **SPK Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**RG_AUDIVLMUTE_VAUDP12**	**RG_AUDIVLMUXSEL_VAUDP12**			**RG_AUDIVLSTARTUP_VAUDP12**	**RG_AUDIVLPWRUP_VAUDP12**				
Type							RW	RW			RW	RW				
Reset							0	0	0	0	0	0				

Bit(s)	Name	Description
9	RG_AUDIVLMUTE_VAUDP12	**Enables audio left channel I-V buffer mute**
8:6	RG_AUDIVLMUXSEL_VAUDP12	**Selects audio left channel IV buffer mux** Positive/negative pins: 000: Open/Open 001: FM stereo mode 010: FM mono mode 011: Open/Open 100: Audio playback mode 101: Audio + FM stereo mode 110: Audio + FM mono mode 111: Audio playback mode
5	RG_AUDIVLSTARTUP_VAUDP12	**Enables audio left channel I-V buffer startup**
4	RG_AUDIVLPWRUP_VAUDP12	**Powers up audio left channel I-V buffer**

0310 **ISINK0_CON0** **ISINK0 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ISINK_DIM0_FSEL**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM0_FSEL	**ISINK0 dimming frequency selection** backlight: (@ 2MHz) 2: 20k Hz 61: 1k Hz 311: 200 Hz 12499: 5 Hz

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Bit(s)	Name	Description
		31249: 2 Hz 62499: 1Hz indicator: (@32KHz) 0: 1k Hz 4: 200 Hz 199: 5 Hz 499: 2 Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2 Hz 9999: 0.1 Hz

0312 ISINK0_CON1 ISINK0 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH0_STEP			ISINK_DIM0_DUTY											
Type		RW			RW											
Reset		0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
14:12	ISINK_CH0_STEP	**Coarse 6 step current level for ISINK CH0** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
11:7	ISINK_DIM0_DUTY	**ISINK ON-duty of dimming0 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32

0314 ISINK0_CON2 ISINK0 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH0_TR1_SEL				ISINK_BREATH0_TR2_SEL				ISINK_BREATH0_TF1_SEL				ISINK_BREATH0_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH0_TR1_SEL	**ISINK0 breath mode rising time selection for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s

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Bit(s)	Name	Description
		8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	ISINK_BREATH0_TR2_SEL	**ISINK0 breath mode rising time selection for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH0_TF1_SEL	**ISINK0 breath mode falling time selection for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH0_TF2_SEL	**ISINK0 breath mode falling time selection for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

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0316 ISINK0_CON3 ISINK0 Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_BREATH0_TON_SEL								ISINK_BREATH0_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH0_TON_SEL	**ISINK0 breath mode Ton time selection** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH0_TOFF_SEL	**ISINK0 breath mode Toff time selection** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0318 ISINK1_CON0 ISINK1 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM1_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM1_FSEL	**ISINK1 dimming frequency selection** backlight: (@ 2MHz) 2: 20k Hz 61: 1k Hz 311: 200 Hz

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Bit(s)	Name	Description
		12499: 5 Hz 31249: 2 Hz 62499: 1Hz indicator: (@32KHz) 0: 1k Hz 4: 200 Hz 199: 5 Hz 499: 2 Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2 Hz 9999: 0.1 Hz

031A ISINK1_CON1 ISINK1 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH1_STEP			ISINK_DIM1_DUTY											
Type		RW			RW											
Reset		0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
14:12	ISINK_CH1_STEP	**Coarse 6 step current level for ISINK CH1** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
11:7	ISINK_DIM1_DUTY	**ISINK ON-duty of dimming1 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32

031C ISINK1_CON2 ISINK1 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH1_TR1_SEL				ISINK_BREATH1_TR2_SEL				ISINK_BREATH1_TF1_SEL				ISINK_BREATH1_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH1_TR1_SEL	**ISINK1 breath mode rising time selection for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s

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Bit(s)	Name	Description
		8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	ISINK_BREATH1_TR2_SEL	**ISINK1 breath mode rising time selection for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH1_TF1_SEL	**ISINK1 breath mode falling time selection for duty 0% ~ 30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH1_TF2_SEL	**ISINK1 breath mode falling time selection for duty31% ~ 100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

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031E ISINK1_CON3 ISINK1 Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_BREATH1_TON_SEL								ISINK_BREATH1_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH1_TON_SEL	**ISINK1 breath mode Ton time selection** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH1_TOFF_SEL	**ISINK1 breath mode Toff time selection** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0324 ISINK_SFSTR ISINK SOFT START 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_SFSTR0_TC		ISINK_SFSTR0_EN		ISINK_SFSTR1_TC		ISINK_SFSTR1_EN								
Type		RW		RW		RW		RW								
Reset		0	0	0		0	0	0								

Bit(s)	Name	Description
14:13	ISINK_SFSTR0_TC	**isink0 soft start timing step control** freq: 2MHz

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Bit(s)	Name	Description
		2'b00: 1T (0.5us) 2'b01: 2T (1us) 2'b10: 3T (1.5us) 2'b11: 4T (2us)
12	ISINK_SFSTR0_EN	**isink0 soft start control** 1'b1: enable sfter start current step 1'b0: disable
10:9	ISINK_SFSTR1_TC	**isink1 soft start timing step control** freq: 2MHz 2'b00: 1T (0.5us) 2'b01: 2T (1us) 2'b10: 3T (1.5us) 2'b11: 4T (2us)
8	ISINK_SFSTR1_EN	**isink1 soft start control** 1'b1: enable sfter start current step 1'b0: disable

0326 **ISINK_EN_CTRL** **ISINK Enable control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ISINK_CH1_BIAS_EN	ISINK_CH0_BIAS_EN			ISINK_CHOP1_EN	ISINK_CHOP0_EN			ISINK_CH1_EN	ISINK_CH0_EN
Type							RW	RW			RW	RW			RW	RW
Reset							0	0			0	0			0	0

Bit(s)	Name	Description
9	ISINK_CH1_BIAS_EN	**ISINK Channel 1 CHOP CLK enable** 1'b0: Disable 1'b1: Enable
8	ISINK_CH0_BIAS_EN	**ISINK Channel 0 CHOP CLK enable** 1'b0: Disable 1'b1: Enable
5	ISINK_CHOP1_EN	**ISINK Channel 1 CHOP CLK enable** 1'b0: Disable 1'b1: Enable
4	ISINK_CHOP0_EN	**ISINK Channel 0 CHOP CLK enable** 1'b0: Disable 1'b1: Enable
1	ISINK_CH1_EN	**Turn on ISINK Channel 1** 1'b0: Disable 1'b1: Enable
0	ISINK_CH0_EN	**Turn on ISINK Channel 0** 1'b0: Disable 1'b1: Enable

0328 **ISINK_MODE_CTRL** **ISINK mode control** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_CH0_MODE		ISINK_CH1_MODE													
Type	RW		RW													
Reset	0	0	0	0												

Bit(s)	Name	Description
15:14	ISINK_CH0_MODE	**ISINK Channel 0 enable mode select** 2'b00: PWM mode 2'b01: Breath mode 2'b10: register mode 2'b11: register mode
13:12	ISINK_CH1_MODE	**ISINK Channel 1 enable mode select** 2'b00: PWM mode 2'b01: Breath mode 2'b10: register mode 2'b11: register mode

032A **ISINK_ANA_CON0** **ISINK control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DA_QI_ISINKS_CH0_STEP			DA_QI_ISINKS_CH1_STEP			DA_QI_ISINKS_CH2_STEP			DA_QI_ISINKS_CH3_STEP		
Type					RO			RO			RO			RO		
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:9	DA_QI_ISINKS_CH0_STEP	**Coarse 6 step current level for ISINK CH5,** 000:4mA 001:8mA 010:12mA 011:16mA 100:20mA 101:24mA 110:24mA 111: 24mA
8:6	DA_QI_ISINKS_CH1_STEP	**Coarse 6 step current level for ISINK CH4,** 000:4mA 001:8mA 010:12mA 011:16mA 100:20mA 101:24mA 110:24mA 111: 24mA
5:3	DA_QI_ISINKS_CH2_STEP	**Coarse 6 step current level for ISINK CH1,** 000:4mA 001:8mA 010:12mA 011:16mA 100:20mA 101:24mA 110:24mA 111: 24mA
2:0	DA_QI_ISINKS_CH3	**Coarse 6 step current level for ISINK CH0,**

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Bit(s)	Name	Description
	_STEP	000:4mA 001:8mA 010:12mA 011:16mA 100:20mA 101:24mA 110:24mA 111: 24mA

0334 CHRIND_CON0 CHRIND Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHRIND_DIM_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CHRIND_DIM_FSEL	**ISINK0 dimming frequency selection** backlight: (@ 2MHz) 2: 20k Hz 61: 1k Hz 311: 200 Hz 12499: 5 Hz 31249: 2 Hz 62499: 1Hz indicator: (@32KHz) 0: 1k Hz 4: 200 Hz 199: 5 Hz 499: 2 Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2 Hz 9999: 0.1 Hz

0336 CHRIND_CON1 CHRIND Control Register 1 3000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		CHRIND_STEP			CHRIND_DIM_DUTY											
Type		RW			RW											
Reset		0	1	1	0	0	0	0	0							

Bit(s)	Name	Description
14:12	CHRIND_STEP	**Coarse 6 step current level for chrind** 000: 2mA 001: 4mA 010: 4mA 011: 6mA 100: NA 101: NA 110: NA 111: NA

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Bit(s)	Name	Description
11:7	CHRIND_DIM_DUTY	**ISINK ON-duty of dimming0 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32

0338 **CHRIND_CON2** **CHRIND Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHRIND_BREATH_TR1_SEL				CHRIND_BREATH_TR2_SEL				CHRIND_BREATH_TF1_SEL				CHRIND_BREATH_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	CHRIND_BREATH_TR1_SEL	**CHRIND breath mode rising time selection for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	CHRIND_BREATH_TR2_SEL	**CHRIND breath mode rising time selection for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	CHRIND_BREATH_TF1_SEL	**CHRIND breath mode falling time selection for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s

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Bit(s)	Name	Description
		5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	CHRIND_BREATH_TF2_SEL	**ISINK0 breath mode falling time selection for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

033A **CHRIND_CON3** **CHRIND Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					CHRIND_BREATH_TON_SEL								CHRIND_BREATH_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	CHRIND_BREATH_TON_SEL	**CHRIND breath mode Ton time selection** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	CHRIND_BREATH_T	**CHRIND breath mode Toff time selection**

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Bit(s)	Name	Description
	OFF_SEL	0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

033C **CHRIND_EN_CTRL** **CHRIND Enable control simple** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**CHRIND_BIAS_EN**		**CHRIND_MODE**		**CHRIND_CHOP_EN**	**CHRIND_EN**	**CHRIND_EN_SEL**	**CHRIND_SFSTR_TC**		**CHRIND_SFSTR_EN**
Type							RW		RW		RW	RW	RW	RW		RW
Reset							0		0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	CHRIND_BIAS_EN	**ISINK Channel 2 bias CLK enable** 1'b0: Disable 1'b1: Enable
7:6	CHRIND_MODE	**ISINK Channel 1 enable mode select** 2'b00: PWM mode 2'b01: Breath mode 2'b10: register mode 2'b11: register mode
5	CHRIND_CHOP_EN	**ISINK Channel 3 CHOP CLK enable** 1'b0: Disable 1'b1: Enable
4	CHRIND_EN	**Turn on ISINK Channel 2** 1'b0: Disable 1'b1: Enable
3	CHRIND_EN_SEL	1'b0: auto 1'b1: SW
2:1	CHRIND_SFSTR_TC	**isink3 soft start timing step control** freq: 2MHz 2'b00: 1T (0.5us) 2'b01: 2T (1us) 2'b10: 3T (1.5us) 2'b11: 4T (2us)
0	CHRIND_SFSTR_EN	**isink3 soft start control** 1'b1: enable sfter start current step 1'b0: disable

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041E	BUCK_OC_CON0	BUCK_OC control register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												BUCK_VPA_OC_STATUS	BUCK_VS1_OC_STATUS	BUCK_VPROC_OC_STATUS	BUCK_VCORE2_OC_STATUS	BUCK_VCORE_OC_STATUS
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	BUCK_VPA_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs
3	BUCK_VS1_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs
2	BUCK_VPROC_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs
1	BUCK_VCORE2_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs
0	BUCK_VCORE_OC_STATUS	**OC status condition (write 1 clear)** 0: No OC 1: OC occurs

0424	BUCK_OC_CON3	BUCK_OC control register 3	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												BUCK_VPA_OC_FLAG_CLR	BUCK_VS1_OC_FLAG_CLR	BUCK_VPROC_OC_FLAG_CLR	BUCK_VCORE2_OC_FLAG_CLR	BUCK_VCORE_OC_FLAG_CLR
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	BUCK_VPA_OC_FLAG_CLR	**1: clear OC status** 0: keep OC status
3	BUCK_VS1_OC_FLAG_CLR	**1: clear OC status** 0: keep OC status
2	BUCK_VPROC_OC_FLAG_CLR	**1: clear OC status** 0: keep OC status
1	BUCK_VCORE2_OC_FLAG_CLR	**1: clear OC status** 0: keep OC status
0	BUCK_VCORE_OC_F	**1: clear OC status**

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Bit(s)	Name	Description
	LAG_CLR	0: keep OC status

0426 **BUCK_OC_CON4** **BUCK_OC control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												BUCK_VPA_OC_FLAG_CLR_SEL	BUCK_VS1_OC_FLAG_CLR_SEL	BUCK_VPROC_OC_FLAG_CLR_SEL	BUCK_VCORE2_OC_FLAG_CLR_SEL	BUCK_VCORE_OC_FLAG_CLR_SEL
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	BUCK_VPA_OC_FLAG_CLR_SEL	**1: SW clear OC status** 0: HW clear OC status
3	BUCK_VS1_OC_FLAG_CLR_SEL	**1: SW clear OC status** 0: HW clear OC status
2	BUCK_VPROC_OC_FLAG_CLR_SEL	**1: SW clear OC status** 0: HW clear OC status
1	BUCK_VCORE2_OC_FLAG_CLR_SEL	**1: SW clear OC status** 0: HW clear OC status
0	BUCK_VCORE_OC_FLAG_CLR_SEL	**1: SW clear OC status** 0: HW clear OC status

0432 **SMPS_TOP_ANA_CON0** **SMPS_TOP control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VSRAM_PROC_TRIMH					RG_SMPS_TESTMODE_B								
Type			RW					RW								
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:9	RG_VSRAM_PROC_TRIMH	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV

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Bit(s)	Name	Description
		00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
8:0	RG_SMPS_TESTMODE_B	**Test mode enable bit, Default 0 disable testmode; (default) NORMAL: 8'b00000000** [0]: 0: VBUF GOOD 1: VBUF not good [3:1]: N/A [4] CSM measure from LDO bist 0: no value 1: CSM from LDO bist [7:5]: CSM measurement selection 000: N/A 001: VCORE2 010: VCORE 011: N/A 100: N/A 101: VPROC 110: VS1 111: N/A [8]: pass CSM signal to KP_LED or AUXADC 0: disable 1: enable

0434 **SMPS_TOP_ANA_CON1** **SMPS_TOP control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VPROC_TRIML					RG_VPROC_TRIMH					RG_VSRAM_PROC_TRIML				
Type		RW					RW					RW				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	RG_VPROC_TRIML	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV

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Bit(s)	Name	Description
		10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
9:5	RG_VPROC_TRIMH	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
4:0	RG_VSRAM_PROC_TRIML	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV

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Bit(s)	Name	Description
		11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV

0436 **SMPS_TOP_ANA_CON2** **SMPS_TOP control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VCORE2_TRIMH					RG_VCORE_TRIML					RG_VCORE_TRIMH				
Type		RW					RW					RW				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	RG_VCORE2_TRIMH	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV

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Bit(s)	Name	Description
		00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
9:5	RG_VCORE_TRIML	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
4:0	RG_VCORE_TRIMH	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV

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Bit(s)	Name	Description
		00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV

0438 **SMPS_TOP_ANA_CON3** **SMPS_TOP control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VS1_TRIML				RG_VS1_TRIMH				RG_VCORE2_TRIML				
Type				RW				RW				RW				
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:9	RG_VS1_TRIML	**R2R DAC reference fine tune** 1111: Vo offset=+6.25mV 1110: Vo offset=+12.5mV 1101: Vo offset=+18.75mV 1100: Vo offset=+25mV 1011: Vo offset=+31.25mV 1010: Vo offset=+37.5mV 1001: Vo offset=+43.75mV 0000: Vo offset=0mV (default) 0001: Vo offset=-6.25mV 0010: Vo offset=-12.5mV 0011: Vo offset=-18.75mV 0100: Vo offset=-25mV 0101: Vo offset=-31.25mV 0110: Vo offset=-37.5mV 0111: Vo offset=-43.75mV 1000: Vo offset=-50mV
8:5	RG_VS1_TRIMH	**R2R DAC reference fine tune** 1111: Vo offset=+6.25mV 1110: Vo offset=+12.5mV 1101: Vo offset=+18.75mV 1100: Vo offset=+25mV 1011: Vo offset=+31.25mV 1010: Vo offset=+37.5mV 1001: Vo offset=+43.75mV 0000: Vo offset=0mV (default) 0001: Vo offset=-6.25mV 0010: Vo offset=-12.5mV 0011: Vo offset=-18.75mV 0100: Vo offset=-25mV 0101: Vo offset=-31.25mV

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Bit(s)	Name	Description
		0110: Vo offset=-37.5mV 0111: Vo offset=-43.75mV 1000: Vo offset=-50mV
4:0	RG_VCORE2_TRIML	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV

043A **SMPS_TOP_ANA_CON4** **SMPS_TOP control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VPA_TRIM_REF					RG_VPA_TRIML					RG_VPA_TRIMH				
Type		RW					RW					RW				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	RG_VPA_TRIM_REF	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV

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Bit(s)	Name	Description
		10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
9:5	RG_VPA_TRIML	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
4:0	RG_VPA_TRIMH	**R2R DAC reference fine tune** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV

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Bit(s)	Name	Description
		11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV

043C **SMPS_TOP_ANA_CON5** **SMPS_TOP control register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VPA_BURSTL		RG_VPA_BURSTH		RG_VCORE2_VSLEEP			RG_VCORE_VSLEEP			RG_VPROC_VSLEEP			RG_VSRAM_PROC_VSLEEP		
Type	RW		RW		RW			RW			RW			RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_VPA_BURSTL	**PWM/BURST threshold** 00: VH=0.35V (default) 01: VH=0.30V 10: VH=0.40V 11: VH=0.45V
13:12	RG_VPA_BURSTH	**PWM/BURST threshold** 00: VH=0.50V (default) 01: VH=0.45V 10: VH=0.55V 11: VH=0.60V
11:9	RG_VCORE2_VSLEEP	**sleep mode voltage selection** 000: VSLEEP 001: VSLEEP - 12.5mV 010: VSLEEP - 12.5mV*2 011: VSLEEP - 12.5mV*3 100: VSLEEP + 12.5mV*4 101: VSLEEP + 12.5mV*3 110: VSLEEP + 12.5mV*2 111: VSLEEP + 12.5mV
8:6	RG_VCORE_VSLEEP	**sleep mode voltage selection**

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Bit(s)	Name	Description
		000: VSLEEP 001: VSLEEP - 12.5mV 010: VSLEEP - 12.5mV*2 011: VSLEEP - 12.5mV*3 100: VSLEEP + 12.5mV*4 101: VSLEEP + 12.5mV*3 110: VSLEEP + 12.5mV*2 111: VSLEEP + 12.5mV
5:3	RG_VPROC_VSLEEP	**sleep mode voltage selection** 000: VSLEEP 001: VSLEEP - 12.5mV 010: VSLEEP - 12.5mV*2 011: VSLEEP - 12.5mV*3 100: VSLEEP + 12.5mV*4 101: VSLEEP + 12.5mV*3 110: VSLEEP + 12.5mV*2 111: VSLEEP + 12.5mV
2:0	RG_VSRAM_PROC_VSLEEP	**sleep mode voltage selection** 000: VSLEEP 001: VSLEEP - 12.5mV 010: VSLEEP - 12.5mV*2 011: VSLEEP - 12.5mV*3 100: VSLEEP + 12.5mV*4 101: VSLEEP + 12.5mV*3 110: VSLEEP + 12.5mV*2 111: VSLEEP + 12.5mV

043E **SMPS_TOP_ANA_CON6** **SMPS_TOP control register 6** **07F8**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VCORE2_VSLEEP_VOLTAGE		RG_VCORE_VSLEEP_VOLTAGE		RG_VPROC_VSLEEP_VOLTAGE		RG_VSRAM_PROC_VSLEEP_VOLTAGE		RG_DMY100MA_SEL		RG_DMY100MA_EN
Type						RW		RW		RW		RW		RW		RW
Reset						1	1	1	1	1	1	1	1	0	0	0

Bit(s)	Name	Description
10:9	RG_VCORE2_VSLEEP_VOLTAGE	**sleep mode voltage selection** 00: 0.85V 01: 0.90V 10: 0.75V 11: 0.70V
8:7	RG_VCORE_VSLEEP_VOLTAGE	**sleep mode voltage selection** 00: 0.85V 01: 0.90V 10: 0.75V 11: 0.70V
6:5	RG_VPROC_VSLEEP_VOLTAGE	**sleep mode voltage selection** 00: 0.85V 01: 0.90V 10: 0.75V 11: 0.70V
4:3	RG_VSRAM_PROC_VSLEEP_VOLTAGE	**sleep mode voltage selection** 00: 0.7V

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Bit(s)	Name	Description
		01: 0.75V 10: 0.65V 11: 0.6V
2:1	RG_DMY100MA_SEL	**PWM/BURST threshold** 00: typ Iload (default) 01: 10/8 10: 6/8 11: 4/8
0	RG_DMY100MA_EN	**sleep mode voltage selection** 0: DMY load off 1: DMY load on

0440 **VPA_ANA_CON0** **VPA control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VPA_SLP		RG_VPA_CSL		RG_VPA_CSMIR		RG_VPA_CSR		RG_VPA_CC		RG_VPA_RZSEL	
Type					RW		RW		RW		RW		RW		RW	
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:10	RG_VPA_SLP	**slope compensation adjustment** 00: 2.5uA 01: 3.5uA 10: 4uA 11: 5uA
9:8	RG_VPA_CSL	**over current limit adjustment** 00: 1.6A 01: 1.2A 10: 2.0A 11: 2.4A
7:6	RG_VPA_CSMIR	**00: 1.25X** 01: 1.625X 10: 1X 11: 1.375X
5:4	RG_VPA_CSR	**current sense ratio adjustment** 00: 1x (default) 01: 0.5x 10: 1.25x 11: 0.75x
3:2	RG_VPA_CC	**compensation C adjustment** 00: 8pF (default) 01: 6pF 10: 3pF 11: 1pF
1:0	RG_VPA_RZSEL	**compensation R adjustment** 00: 710kohm 01: 610kohm 10: 810kohm 11: 910kohm

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0442 **VPA_ANA_CON1** **VPA control register 1** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VPA_NDIS_EN	RG_VPA_SLEW_NMOS		RG_VPA_SLEW		RG_VPA_MODESET	RG_VPA_BWEX_GAT	RG_VPA_HZP	RG_VPA_ZX_OS		RG_VPA_ZX_OS_TRIM					
Type	RW	RW		RW		RW	RW	RW	RW		RW					
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_VPA_NDIS_EN	**POWER DOWN NMOS Enable** 1: enable (default) (with pull-low) 0: disable (without pull-low)
14:13	RG_VPA_SLEW_NMOS	**lgate slew rate control** 00: ~1ns (default) 01: ~2ns 10: ~5ns 11: ~10ns
12:11	RG_VPA_SLEW	**ugate slew rate control** 00: ~1ns (default) 01: ~2ns 10: ~5ns 11: ~10ns
10	RG_VPA_MODESET	**1: force PWM mode** 0: auto mode
9	RG_VPA_BWEX_GAT	**BW extension function gating** 0: BW extension ON (default) 1: BW extension OFF
8	RG_VPA_HZP	**HZ prevention function gating** 0: HZ prevention ON (default) 1: HZ prevention OFF
7:6	RG_VPA_ZX_OS	**Positive offset adjustment for LX zero-crossing detection** 00: +200mV (default) 01: +150mV 10: +250mV 11: +300mV
5:0	RG_VPA_ZX_OS_TRIM	**offset adjustment for LX zero-crossing detection** 0000: -200mV (default) 0001: -150mV 0010: -250mV 0011: -300mV ~ 1101: -800mV 1111:-850mV

0444 **VPA_ANA_CON2** **VPA control register 2** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VPA_RSV1									RG_VPA_VBAT_DEL		RG_VPA_MIN_ON	
Type				RW									RW		RW	
Reset				0	0	0	0	0	0	0	0		0	0	1	0

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Bit(s)	Name	Description
12:5	RG_VPA_RSV1	**RG_VPA_RSV[0]: BW extension gating** RG_VPA_RSV[4:1]: Zero crossing detection point adjustment RG_VPA_RSV[5]: HZ prevention gating RG_VPA_RSV[6]: CS adjustment
3:2	RG_VPA_VBAT_DEL	**Lowdrop out threshold detection** 00: VR=0.6V (default) 01: VR=0.55V 10: VR=0.65V 11: VR=0.70V
1:0	RG_VPA_MIN_ON	

0446 **VPA_ANA_CON3** **VPA control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RGS_VPA_ZX_STATUS	RG_VPA_RSV2							
Type								RO	RW							
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	RGS_VPA_ZX_STATUS	**Zero Cross STATUS**
7:0	RG_VPA_RSV2	**RG_VPA_RSV[0]: BW extension gating** RG_VPA_RSV[4:1]: Zero crossing detection point adjustment RG_VPA_RSV[5]: HZ prevention gating RG_VPA_RSV[6]: CS adjustment

0448 **VCORE_ANA_CON0** **VCORE control register 0** **32A2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VCORE_CSL				RG_VCORE_CSR			RG_VCORE_RZSEL			RG_VCORE_1P35UP_SEL_EN	RG_VCORE_VRF18_SSTART_EN	RG_VCORE_MIN_OFF	
Type			RW				RW			RW			RW	RW	RW	
Reset			1	1	0	0	1	0	1	0	1	0	0	0	1	0

Bit(s)	Name	Description
13:10	RG_VCORE_CSL	**Over current limit adjustment** 4'b0000: 8A 4'b1000: 7A 4'b1100: 6A (default) 4'b1110: 5A 4'b1111: 4A
9:7	RG_VCORE_CSR	**Current sense ratio adjustment** 3'b000: 15.75K 233mV/A

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Bit(s)	Name	Description
		3'b001: 13.5K 200mV/A 3'b010: 11.25K 167mV/A 3'b011: 9K 133mV/A 3'b100: 6.75K(default) 100mV/A 3'b101: 4.5K 67mV/A 3'b110: 2.25K 33mV/A 3'b111: 0K
6:4	RG_VCORE_RZSEL	**Compensation R adjustment** 3'b000: 400 kohm 3'b001: 500 kohm 3'b010: 600 kohm (default) 3'b011: 700 kohm 3'b100: 800 kohm 3'b101: 1000 kohm 3'b110: 1100 kohm 3'b111: 1200 kohm
3	RG_VCORE_1P35UP_SEL_EN	**vo>=1.35v** 1'b0: vo<1.35V, valley current sense 1'b1: vo>=1.35V, peak current sense
2	RG_VCORE_VRF18_SSTART_EN	**no used**
1:0	RG_VCORE_MIN_OFF	**no used**

044A **VCORE_ANA_CON1** **VCORE control register 1** **101A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCORE_NDIS_EN	RG_VCORE_MODESET	RG_VCORE_ZXOS_TRIM						RG_VCORE_ZX_OS		RG_VCORE_SLP		
Type				RW	RW	RW						RW		RW		
Reset				1	0	0	0	0	0	0	0	1	1	0	1	0

Bit(s)	Name	Description
12	RG_VCORE_NDIS_EN	**NMOS discharge Enable** 1'b1: enable NMOS discharge (default) 1'b0: disable NMOS discharge
11	RG_VCORE_MODESET	**Force PWM mode select** 1'b1: force PWM mode 1'b0: auto mode
10:5	RG_VCORE_ZXOS_TRIM	**1LSB=260mA** LX zero-crossing offset trimming 6'b000001: +1LSB 6'b000010: +2LSB 6'b000100: +4LSB 6'b001000: -1LSB 6'b010000: -2LSB 6'b100000: -4LSB
4:3	RG_VCORE_ZX_OS	**Nlim trimimg bits(combined with RG_VCORE_RSV[7],[6], as RG_VCORE_RSV[7],[6],zx_os[1],[0])** 2'b0100: -5m 2'b 1000: -1.66

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Bit(s)	Name	Description
		2'b1110: -1.74 2'b1101: -1.62 2'b1100:-1.5
2:0	RG_VCORE_SLP	**slope compensation adjustment** 3'b000: 1uA 3'b001: 1.5uA 3'b010: 2uA (default) 3'b011: 2.5uA 3'b100: 3uA 3'b101: 3.5uA 3'b110: 4uA 3'b111: 4.5uA

044C **VCORE_ANA_CON2** **VCORE control register 2** **0820**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCORE_CSM_P						RG_VCORE_CSM_N					
Type					RW						RW					
Reset					1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
11:6	RG_VCORE_CSM_P	**current measure adjustment** [0]: IMAX=1.5V OR 1V 1b'0: 1.5 V 1b'1: 1V [5]: Test peak/valley current 1'b0: valley 1'b1:peak 6'bX0000X : +0% 6'bX0001X : -3% 6'bX0010X : -6% 6'bX0011X : -9% 6'bX0100X : -12% 6'bX0101X : -15% 6'bX0110X : -18% 6'bX0111X : -21% 6'bX1000X : +24% 6'bX1001X : +21% 6'bX1010X : +18% 6'bX1011X : +15% 6'bX1100X : +12% 6'bX1101X : +9% 6'bX1110X : +6% 6'bX1111X : +3%
5:0	RG_VCORE_CSM_N	**current measure adjustment** [0]: IMAX=1.5V OR 1V 1b'0: 1.5 V 1b'1: 1V [5]: Test Mode enable 1'b0: disable 1'b1:enable 6'bX0000X : +0% 6'bX0001X : -3% 6'bX0010X : -6% 6'bX0011X : -9% 6'bX0100X : -12%

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Bit(s)	Name	Description
		6'bX0101X : -15% 6'bX0110X : -18% 6'bX0111X : -21% 6'bX1000X : +24% 6'bX1001X : +21% 6'bX1010X : +18% 6'bX1011X : +15% 6'bX1100X : +12% 6'bX1101X : +9% 6'bX1110X : +6% 6'bX1111X : +3%

044E **VCORE_ANA_CON3** **VCORE control register 3** **04F0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VCORE_PWM_TRIG	RG_VCORE_AUTO_MODE	RG_VCORE_DTS_ENB	RG_VCORE_PFM_RIP			RG_VCORE_RSV							
Type			RW	RW	RW	RW			RW							
Reset			0	0	0	1	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
13	RG_VCORE_PWM_TRIG	**NA**
12	RG_VCORE_AUTO_MODE	**NA**
11	RG_VCORE_DTS_ENB	**differential to single buffer disable signal**
10:8	RG_VCORE_PFM_RIP	**PFM ripple control bit** 1 LSB=6.25mV 3'b000: +0LSB 3'b001: +1LSB 3'b010: +2LSB 3'b011: +3LSB 3'b100: +4LSB 3'b101: +5LSB 3'b110: +6LSB 3'b111: +7LSB
7:0	RG_VCORE_RSV	**Reserved:** [7]: for nlim trimmimg [6]: for nlim trimmimg [5]: HS on- speed increase [4]:power good function gating 0: check Output drop voltage (COMPARATOR) 1: check NMOS threshold [3]:HS driver detection threshold voltage [2]: VBAT<2.8V, increase Powermos slew rate [1]:nlim gating [0]: in PFM mode, increase slew rate

0450 **VCORE_ANA_** **VCORE control register 4** **000B**

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CON4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_VCORE_ENPWM_STATUS	RG_VCORE_TRAN_BST					
Type										RO	RW					
Reset										0	0	0	1	0	1	1

Bit(s)	Name	Description
6	RGS_VCORE_ENPWM_STATUS	**ENPWM STATUS** H: PWM mode L: PFM mode
5:0	RG_VCORE_TRAN_BST	**PFM -> PWM transient boost EN (1=EN)** [5]: reserved, no used [4]: reserved, no used [3]:reserved, no used [2]:reserved, no used [1]: AVP [0]: BW extension

0452 **VPROC_ANA_CON0** **VPROC control register 0** **22E2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VPROC_CSL				RG_VPROC_CSR			RG_VPROC_RZSEL			RG_VPROC_1P35UP_SEL_EN	RG_VPROC_VRF18_SSTART_EN	RG_VPROC_MIN_OFF	
Type			RW				RW			RW			RW	RW	RW	
Reset			1	0	0	0	1	0	1	1	1	0	0	0	1	0

Bit(s)	Name	Description
13:10	RG_VPROC_CSL	**Over current limit adjustment** 4'b0000: 8A 4'b1000: 7A(default) 4'b1100: 6A 4'b1110: 5A 4'b1111: 4A
9:7	RG_VPROC_CSR	**Current sense ratio adjustment** 3'b000: 15.75K 233mV/A 3'b001: 13.5K 200mV/A 3'b010: 11.25K 167mV/A 3'b011: 9K 133mV/A 3'b100: 6.75K 100mV/A 3'b101: 4.5K (default) 67mV/A 3'b110: 2.25K 33mV/A 3'b111: 0K
6:4	RG_VPROC_RZSEL	**Compensation R adjustment** 3'b000: 400 kohm 3'b001: 800 kohm 3'b010: 1200 kohm 3'b011: 1400 kohm

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Bit(s)	Name	Description
		3'b100: 1500 kohm 3'b101: 1600 kohm 3'b110: 1800 kohm(default) 3'b111: 1900 kohm
3	RG_VPROC_1P35UP_SEL_EN	**vo>=1.35v** 1'b0: vo<1.35V, valley current sense 1'b1: vo>=1.35V, peak current sense
2	RG_VPROC_VRF18_SSTART_EN	**no used**
1:0	RG_VPROC_MIN_OFF	**no used**

0454 VPROC_ANA_CON1 VPROC control register 1 1004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_VPROC_NDIS_EN**	**RG_VPROC_MODESET**	**RG_VPROC_ZXOS_TRIM**						**RG_VPROC_ZX_OS**		**RG_VPROC_SLP**		
Type				RW	RW	RW						RW		RW		
Reset				1	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
12	RG_VPROC_NDIS_EN	**NMOS discharge Enable** 1'b1: enable NMOS discharge (default) 1'b0: disable NMOS discharge
11	RG_VPROC_MODESET	**Force PWM mode select** 1'b1: force PWM mode 1'b0: auto mode
10:5	RG_VPROC_ZXOS_TRIM	**1LSB=260mA** LX zero-crossing offset trimming 6'b000001: +1LSB 6'b000010: +2LSB 6'b000100: +4LSB 6'b001000: -1LSB 6'b010000: -2LSB 6'b100000: -4LSB
4:3	RG_VPROC_ZX_OS	**Nlim trimimg bits(combined with RG_VPROC_RSV[7],[6], as RG_VPROC_RSV[7],[6],zx_os[1],[0])** 2'b0100: -5m 2'b 1000: -1.66 2'b1110: -1.74 2'b1101: -1.62 2'b1100:-1.5
2:0	RG_VPROC_SLP	**slope compensation adjustment** 3'b000: 1uA 3'b001: 1.5uA 3'b010: 2uA 3'b011: 2.5uA 3'b100: 3uA (default) 3'b101: 3.5uA 3'b110: 4uA 3'b111: 4.5uA

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0456 **VPROC_ANA_CON2** **VPROC control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VPROC_CSM_P						RG_VPROC_CSM_N					
Type					RW						RW					
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:6	RG_VPROC_CSM_P	**current measure adjustment** [0]: IMAX=1.5V OR 1V 1b'0: 1.5 V 1b'1: 1V [5]: Test peak/valley current 1'b0: valley 1'b1:peak 6'bX0000X : +0% 6'bX0001X : -3% 6'bX0010X : -6% 6'bX0011X : -9% 6'bX0100X : -12% 6'bX0101X : -15% 6'bX0110X : -18% 6'bX0111X : -21% 6'bX1000X : +24% 6'bX1001X : +21% 6'bX1010X : +18% 6'bX1011X : +15% 6'bX1100X : +12% 6'bX1101X : +9% 6'bX1110X : +6% 6'bX1111X : +3%
5:0	RG_VPROC_CSM_N	**current measure adjustment** [0]: IMAX=1.5V OR 1V 1b'0: 1.5 V 1b'1: 1V [5]: Test Mode enable 1'b0: disable 1'b1:enable 6'bX0000X : +0% 6'bX0001X : -3% 6'bX0010X : -6% 6'bX0011X : -9% 6'bX0100X : -12% 6'bX0101X : -15% 6'bX0110X : -18% 6'bX0111X : -21% 6'bX1000X : +24% 6'bX1001X : +21% 6'bX1010X : +18% 6'bX1011X : +15% 6'bX1100X : +12% 6'bX1101X : +9% 6'bX1110X : +6% 6'bX1111X : +3%

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0458 **VPROC_ANA_CON3** **VPROC control register 3** **04F0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VPROC_PWM_TRIG	RG_VPROC_BW_EXTEND	RG_VPROC_DTS_ENB	RG_VPROC_PFM_RIP			RG_VPROC_RSV							
Type			RW	RW	RW	RW			RW							
Reset			0	0	0	1	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
13	RG_VPROC_PWM_TRIG	**NA**
12	RG_VPROC_BW_EXTEND	**enlarge loop bandwidth** 1'b0: default (Cout=47uF*3) 1'b1: extend loop bandwidth (Cout=47uF*4)
11	RG_VPROC_DTS_ENB	**differential to single buffer disable signal**
10:8	RG_VPROC_PFM_RIP	**PFM ripple control bit** 1 LSB=6.25mV 3'b000: +0LSB 3'b001: +1LSB 3'b010: +2LSB 3'b011: +3LSB 3'b100: +4LSB 3'b101: +5LSB 3'b110: +6LSB 3'b111: +7LSB
7:0	RG_VPROC_RSV	**Reserved:** [7]: for nlim trimmimg [6]: for nlim trimmimg [5]: HS on- speed increase [4]:power good function gating 0: check Output drop voltage (COMPARATOR) 1: check NMOS threshold [3]:HS driver detection threshold voltage [2]: VBAT<2.8V, increase Powermos slew rate [1]:nlim gating [0]: in PFM mode, increase slew rate

045A **VPROC_ANA_CON4** **VPROC control register 4** **000B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_VPROC_ENPWM_STATUS	RG_VPROC_TRAN_BST					
Type										RO	RW					
Reset										0	0	0	1	0	1	1

Bit(s)	Name	Description
6	RGS_VPROC_ENPW	**ENPWM STATUS**

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Bit(s)	Name	Description
	M_STATUS	H: PWM mode L: PFM mode
5:0	RG_VPROC_TRAN_BST	**PFM -> PWM transient boost EN (1=EN)** [5]: reserved, no used [4]: reserved, no used [3]:reserved, no used [2]:reserved, no used [1]: AVP [0]: BW extension

045C **VS1_ANA_CON0** **VS1 control register 0** **6312**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VS1_CSL				RG_VS1_CSR			RG_VS1_RZSEL			RG_VS1_1P35UP_SEL_EN	RG_VS1_VRF18_SSTART_EN	RG_VS1_NVT_BUFF_OFF_EN	RG_VS1_MIN_OFF	
Type		RW				RW			RW			RW	RW	RW	RW	
Reset		1	1	0	0	0	1	1	0	0	0	1	0	0	1	0

Bit(s)	Name	Description
14:11	RG_VS1_CSL	**Over current limit adjustment** 4'b0000: 1.2A 4'b1000: 2A 4'b1100: 3A (Default) 4'b1110: 4A 4'b1111: 4.8A
10:8	RG_VS1_CSR	**Current sense ratio adjustment** 3'b000: 234mV 3'b001: 208mV 3'b010: 182mV 3'b011: 156mV (Default) 3'b100: 130mV 3'b101: 104mV 3'b110: 78mV 3'b111: 52mV
7:5	RG_VS1_RZSEL	**Compensation R adjustment** 3'b000: 700 kohm (Default) 3'b001: 300 kohm 3'b010: 200 kohm 3'b011: 500 kohm 3'b100: 800 kohm 3'b101: 900 kohm 3'b110: 1000 kohm 3'b111: 1200 kohm
4	RG_VS1_1P35UP_SEL_EN	**Vo>=1.35v select** 1'b0: Vo<1.35v 1'b1: Vo>=1.35v
3	RG_VS1_VRF18_SSTART_EN	**VS1 soft-start time enable** 1'b0: disable 1'b1: enable
2	RG_VS1_NVT_BUFF_OFF_EN	**no-used**

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Bit(s)	Name	Description
1:0	RG_VS1_MIN_OFF	**no-used**

045E **VS1_ANA_CON1** **VS1 control register 1** **0021**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_VS1_CSM_N**						**RG_VS1_NDIS_EN**	**RG_VS1_ZX_OS**		**RG_VS1_SLP**		
Type					RW						RW	RW		RW		
Reset					0	0	0	0	0	0	1	0	0	0	0	1

Bit(s)	Name	Description
11:6	RG_VS1_CSM_N	**current measure adjustment** 5'b00000 : +0% 5'b00001 : -3% 5'b00010 : -6% 5'b00011 : -9% 5'b00100 : -12% 5'b00101 : -15% 5'b00110 : -18% 5'b00111 : -21% 5'b01000 : +24% 5'b01001 : +21% 5'b01010 : +18% 5'b01011 : +15% 5'b01100 : +12% 5'b01101 : +9% 5'b01110 : +6% 5'b01111 : +3%
5	RG_VS1_NDIS_EN	**NMOS discharge Enable** 1'b1: enable NMOS discharge (default) 1'b0: disable NMOS discharge
4:3	RG_VS1_ZX_OS	**nlim offset adjustment combine with RG_VS1_RSV[7:6]** RG_VS1_RSV[7:6]+RG_VS1_ZX_OS[1:0] 1LSB = 170mA 0001: -1LSB 0010: -2LSB 0100: -4LSB 1000:+8LSB
2:0	RG_VS1_SLP	**slope compensation adjustment** 3'b000: 1uA 3'b001: 1.5uA (Default) 3'b010: 2uA 3'b011: 2.5uA 3'b100: 3uA 3'b101: 3.5uA 3'b110: 4uA 3'b111: 4.5uA

0460 **VS1_ANA_CON2** **VS1 control register 2** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VS1_RSV								RG_VS1_CSM_P					
Type			RW								RW					
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:6	RG_VS1_RSV	**Reserved:** [7]: for nlim trimmimg [6]: for nlim trimmimg [5]: HS on- speed increase [4]: for power good ibias enable [3]: HS driver decection threshold voltage [2]: VBAT<2.8V, increase Powermos slew rate [1]:nlim gating [0]: in PFM mode, increase slew rate
5:0	RG_VS1_CSM_P	**current measure adjustment** 5'b00000 : +0% 5'b00001 : -3% 5'b00010 : -6% 5'b00011 : -9% 5'b00100 : -12% 5'b00101 : -15% 5'b00110 : -18% 5'b00111 : -21% 5'b01000 : +24% 5'b01001 : +21% 5'b01010 : +18% 5'b01011 : +15% 5'b01100 : +12% 5'b01101 : +9% 5'b01110 : +6% 5'b01111 : +3%

0462 **VS1_ANA_CON3** **VS1 control register 3** **2D00**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VS1_TRAN_BST						RG_VS1_PFM_RIP			RG_VS1_MODESET	RG_VS1_ZXOS_TRIM					
Type	RW						RW			RW	RW					
Reset	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:10	RG_VS1_TRAN_BST	**PFM -> PWM transient boost EN (1=EN)** [5]: reserved [4]: droop [3:2]: 00: no preset duty 01: preset duty low 10: preset duty med 11: preset duty high [1]: AVP [0]: BW extension
9:7	RG_VS1_PFM_RIP	**PFM ripple control bit (1LSB=6.25mV)** 3'b000: +0LSB 3'b001: +1LSB 3'b010: +2LSB

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Bit(s)	Name	Description
		3'b011: +3LSB 3'b100: +4LSB 3'b101: +5LSB 3'b110: +6LSB 3'b111: +7LSB
6	RG_VS1_MODESET	**Force PWM mode select** 1'b1: force PWM mode 1'b0: auto mode
5:0	RG_VS1_ZXOS_TRIM	**LX zero-crossing offset trimming** 1LSB=150mA 6'b000001: +1LSB 6'b000010: +2LSB 6'b000100: +4LSB 6'b001000: -1LSB 6'b010000: -2LSB 6'b100000: -4LSB

0464 VS1_ANA_CON4 VS1 control register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**RGS_VS1_ENPWM_STATUS**	**RG_VS1_PWM_TRIG**	**RG_VS1_AUTO_MODE**	**RG_VS1_DTS_ENB**
Type													RO	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RGS_VS1_ENPWM_STATUS	**ENPWM STATUS** H: PWM mode L: PFM mode
2	RG_VS1_PWM_TRIG	**enlarge offset between vref_sw and vref_trig** 1'b1: 4LSB 1'b0: 2LSB
1	RG_VS1_AUTO_MODE	**no-used**
0	RG_VS1_DTS_ENB	**differential to single buffer disable signal**

0466 BUCK_ANA_CON0 BUCK_ANA_CON0 2B33

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**DA_QI_VPROC_BURST**			**DA_QI_VS1_BURST**				**DA_QI_VCORE2_BURST**				**DA_QI_VCORE_BURST**		
Type			RW			RW				RW				RW		
Reset			1	0	1	0	1	1		0	1	1		0	1	1

Bit(s)	Name	Description
13:11	DA_QI_VPROC_BURST	**PFM IPEAK setting** 3'b001:972mA

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Bit(s)	Name	Description
		3'b010: 1110mA 3'b011: 1350mA 3'b100: 1510mA 3'b101: 1770mA 3'b110: 2000mA 3'b111: 2240mA
10:8	DA_QI_VS1_BURST	**PFM IPEAK setting** 3'b001: 600mA 3'b010: 800mA 3'b011: 1000mA 3'b100: 1100mA 3'b101: 1200mA 3'b110: 1300mA 3'b111: 1400mA
6:4	DA_QI_VCORE2_BURST	**PFM IPEAK setting** 3'b001:972mA 3'b010: 1110mA 3'b011: 1350mA 3'b100: 1510mA 3'b101: 1770mA 3'b110: 2000mA 3'b111: 2240mA
2:0	DA_QI_VCORE_BURST	**PFM IPEAK setting** 3'b001:972mA 3'b010: 1110mA 3'b011: 1350mA 3'b100: 1510mA 3'b101: 1770mA 3'b110: 2000mA 3'b111: 2240mA

0468 **BUCK_ANA_CON1** **BUCK_ANA_CON1** **FFFF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VPROC_DLC_N		DA_QI_VPROC_DLC		DA_QI_VS1_DLC_N		DA_QI_VS1_DLC		DA_QI_VCORE2_DLC_N		DA_QI_VCORE2_DLC		DA_QI_VCORE_DLC_N		DA_QI_VCORE_DLC	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:14	DA_QI_VPROC_DLC_N	**LS NMOS off slew rate and driver detection threshold:** [0]: 1'b0: threshold high 1'b1:threshold low [1]: 1'b1: LS NMOS off slew rate fast 1'b0: LS NMOS off slew rate slow
13:12	DA_QI_VPROC_DLC	**HS PMOS off slew rate:** 2'b00:min 2'b01:med 2'b10:med 2'b11:max
11:10	DA_QI_VS1_DLC_N	**LS NMOS off slew rate and driver detection threshold:** [0]: 1'b0: threshold high 1'b1:threshold low

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Bit(s)	Name	Description
		[1]: 1'b1: LS NMOS off slew rate fast 1'b0: LS NMOS off slew rate slow
9:8	DA_QI_VS1_DLC	**HS PMOS off slew rate:** 2'b00:min 2'b01:med 2'b10:med 2'b11:max
7:6	DA_QI_VCORE2_DLC_N	**LS NMOS off slew rate and driver detection threshold:** [0]: 1'b0: threshold high 1'b1:threshold low [1]: 1'b1: LS NMOS off slew rate fast 1'b0: LS NMOS off slew rate slow
5:4	DA_QI_VCORE2_DLC	**HS PMOS off slew rate:** 2'b00:min 2'b01:med 2'b10:med 2'b11:max
3:2	DA_QI_VCORE_DLC_N	**LS NMOS off slew rate and driver detection threshold:** [0]: 1'b0: threshold high 1'b1:threshold low [1]: 1'b1: LS NMOS off slew rate fast 1'b0: LS NMOS off slew rate slow
1:0	DA_QI_VCORE_DLC	**HS PMOS off slew rate:** 2'b00:min 2'b01:med 2'b10:med 2'b11:max

046A **VCORE2_ANA_CON0** **VCORE2 control register 0** **32A2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VCORE2_CSL				RG_VCORE2_CSR			RG_VCORE2_RZSEL			RG_VCORE2_1P35UP_SEL_EN	RG_VCORE2_VRF18_SSTART_EN	RG_VCORE2_MIN_OFF	
Type			RW				RW			RW			RW	RW	RW	
Reset			1	1	0	0	1	0	1	0	1	0	0	0	1	0

Bit(s)	Name	Description
13:10	RG_VCORE2_CSL	**Over current limit adjustment** 4'b0000: 8A 4'b1000: 7A 4'b1100: 6A (default) 4'b1110: 5A 4'b1111: 4A
9:7	RG_VCORE2_CSR	**Current sense ratio adjustment** 3'b000: 15.75K 233mV/A 3'b001: 13.5K 200mV/A 3'b010: 11.25K 167mV/A 3'b011: 9K 133mV/A 3'b100: 6.75K(default) 100mV/A

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Bit(s)	Name	Description
		3'b101: 4.5K 67mV/A 3'b110: 2.25K 33mV/A 3'b111: 0K
6:4	RG_VCORE2_RZSEL	**Compensation R adjustment** 3'b000: 400 kohm 3'b001: 500 kohm 3'b010: 600 kohm (default) 3'b011: 700 kohm 3'b100: 800 kohm 3'b101: 1000 kohm 3'b110: 1100 kohm 3'b111: 1200 kohm
3	RG_VCORE2_1P35UP_SEL_EN	**vo>=1.35v** 1'b0: vo<1.35V, valley current sense 1'b1: vo>=1.35V, peak current sense
2	RG_VCORE2_VRF18_SSTART_EN	**no used**
1:0	RG_VCORE2_MIN_OFF	**no used**

046C **VCORE2_ANA_CON1** **VCORE2 control register 1** **101A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCORE2_NDIS_EN	RG_VCORE2_MODESET	RG_VCORE2_ZXOS_TRIM						RG_VCORE2_ZX_OS		RG_VCORE2_SLP		
Type				RW	RW	RW						RW		RW		
Reset				1	0	0	0	0	0	0	0	1	1	0	1	0

Bit(s)	Name	Description
12	RG_VCORE2_NDIS_EN	**NMOS discharge Enable** 1'b1: enable NMOS discharge (default) 1'b0: disable NMOS discharge
11	RG_VCORE2_MODESET	**Force PWM mode select** 1'b1: force PWM mode 1'b0: auto mode
10:5	RG_VCORE2_ZXOS_TRIM	**1LSB=260mA** LX zero-crossing offset trimming 6'b000001: +1LSB 6'b000010: +2LSB 6'b000100: +4LSB 6'b001000: -1LSB 6'b010000: -2LSB 6'b100000: -4LSB
4:3	RG_VCORE2_ZX_OS	**Nlim trimimg bits(combined with RG_VCORE2_RSV[7],[6], as RG_VCORE2_RSV[7],[6],zx_os[1],[0])** 2'b0100: -5m 2'b 1000: -1.66 2'b1110: -1.74 2'b1101: -1.62 2'b1100:-1.5
2:0	RG_VCORE2_SLP	**slope compensation adjustment**

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Bit(s)	Name	Description
		3'b000: 1uA 3'b001: 1.5uA 3'b010: 2uA (default) 3'b011: 2.5uA 3'b100: 3uA 3'b101: 3.5uA 3'b110: 4uA 3'b111: 4.5uA

046E **VCORE2_ANA_CON2** **VCORE2 control register 2** **0820**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCORE2_CSM_P						RG_VCORE2_CSM_N					
Type					RW						RW					
Reset					1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
11:6	RG_VCORE2_CSM_P	**current measure adjustment** [0]: IMAX=1.5V OR 1V 1b'0: 1.5 V 1b'1: 1V [5]: Test peak/valley current 1'b0: valley 1'b1:peak 6'bX0000X : +0% 6'bX0001X : -3% 6'bX0010X : -6% 6'bX0011X : -9% 6'bX0100X : -12% 6'bX0101X : -15% 6'bX0110X : -18% 6'bX0111X : -21% 6'bX1000X : +24% 6'bX1001X : +21% 6'bX1010X : +18% 6'bX1011X : +15% 6'bX1100X : +12% 6'bX1101X : +9% 6'bX1110X : +6% 6'bX1111X : +3%
5:0	RG_VCORE2_CSM_N	**current measure adjustment** [0]: IMAX=1.5V OR 1V 1b'0: 1.5 V 1b'1: 1V [5]: Test Mode enable 1'b0: disable 1'b1:enable 6'bX0000X : +0% 6'bX0001X : -3% 6'bX0010X : -6% 6'bX0011X : -9% 6'bX0100X : -12% 6'bX0101X : -15% 6'bX0110X : -18% 6'bX0111X : -21% 6'bX1000X : +24% 6'bX1001X : +21%

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Bit(s)	Name	Description
		6'bX1010X : +18% 6'bX1011X : +15% 6'bX1100X : +12% 6'bX1101X : +9% 6'bX1110X : +6% 6'bX1111X : +3%

0470 VCORE2_ANA_CON3 VCORE2 control register 3 04F0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VCORE2_PWM_TRIG	RG_VCORE2_AUTO_MODE	RG_VCORE2_DTS_ENB	RG_VCORE2_PFM_RIP			RG_VCORE2_RSV							
Type			RW	RW	RW	RW			RW							
Reset			0	0	0	1	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
13	RG_VCORE2_PWM_TRIG	**NA**
12	RG_VCORE2_AUTO_MODE	**NA**
11	RG_VCORE2_DTS_ENB	**differential to single buffer disable signal**
10:8	RG_VCORE2_PFM_RIP	**PFM ripple control bit** 1 LSB=6.25mV 3'b000: +0LSB 3'b001: +1LSB 3'b010: +2LSB 3'b011: +3LSB 3'b100: +4LSB 3'b101: +5LSB 3'b110: +6LSB 3'b111: +7LSB
7:0	RG_VCORE2_RSV	**Reserved:** [7]: for nlim trimmimg [6]: for nlim trimmimg [5]: HS on- speed increase [4]:power good function gating 0: check Output drop voltage (COMPARATOR) 1: check NMOS threshold [3]:HS driver detection threshold voltage [2]: VBAT<2.8V, increase Powermos slew rate [1]:nlim gating [0]: in PFM mode, increase slew rate

0472 VCORE2_ANA_CON4 VCORE2 control register 4 000B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_VCOR	RG_VCORE2_TRAN_BST					

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										E2_ENPWM_STATUS						
Type										RO	RW					
Reset										0	0	0	1	0	1	1

Bit(s)	Name	Description
6	RGS_VCORE2_ENPWM_STATUS	**ENPWM STATUS** H: PWM mode L: PFM mode
5:0	RG_VCORE2_TRAN_BST	**PFM -> PWM transient boost EN (1=EN)** [5]: reserved, no used [4]: reserved, no used [3]:reserved, no used [2]:reserved, no used [1]: AVP [0]: BW extension

0604 **BUCK_VPROC_EN_CON0** **BUCK VPROC ENABLE CON0** **3021**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUCK_VPROC_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	BUCK_VPROC_EN	**Enable control in SW mode**

0608 **BUCK_VPROC_VOL_CON0** **BUCK VPROC VOLTAGE CON0** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DA_NI_VPROC_VOSEL						
Type										RO						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	DA_NI_VPROC_VOSEL	**VOUT selection in binary format**

060A **BUCK_VPROC_VOL_CON1** **BUCK VPROC VOLTAGE CON1** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VPROC_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

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Bit(s)	Name	Description
6:0	BUCK_VPROC_VOSEL	**VOUT selection in SW mode** Voltage = 0.6 + 0.00625 x code

060C **BUCK_VPROC_VOL_CON2** **BUCK VPROC VOLTAGE CON2** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VPROC_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VPROC_VOSEL_ON	**VOUT selection in normal mode when VOSEL configured in HW mode**

0612 **BUCK_VS1_HWM_CON0** **BUCK VS1 HW MODE CON0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DA_VS1_MODESET	BUCK_VS1_MODESET_2	BUCK_VS1_MODESET_1	BUCK_VS1_MODESET_0					
Type								RO	RW	RW	RW					
Reset								0	0	0	0					

Bit(s)	Name	Description
8	DA_VS1_MODESET	
7	BUCK_VS1_MODESET_2	**Force PWM mode select** 1'b1: force PWM mode 1'b0: auto mode
6	BUCK_VS1_MODESET_1	**Force PWM mode select** 1'b1: force PWM mode 1'b0: auto mode
5	BUCK_VS1_MODESET_0	**Force PWM mode select** 1'b1: force PWM mode 1'b0: auto mode

0614 **BUCK_VS1_HWM_CON0_SET** **BUCK_VS1_HWM control register 0_SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUCK_VS1_HWM_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	BUCK_VS1_HWM_CON0_SET	**Set BUCK_VS1_HWM_CON0** 1'b0: no set 1'b1: set

0616 BUCK_VS1_HWM_CON0_CLR BUCK_VS1_HWM control register 0_CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUCK_VS1_HWM_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUCK_VS1_HWM_CON0_CLR	**Clear BUCK_VS1_HWM_CON0** 1'b0: no clear 1'b1: clear

061A BUCK_VS1_EN_CON0 BUCK VS1 ENABLE CON0 3021

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUCK_VS1_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	BUCK_VS1_EN	**Enable control in SW mode**

061E BUCK_VS1_VOL_CON0 BUCK VS1 VOLTAGE CON0 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DA_NI_VS1_VOSEL						
Type										RO						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	DA_NI_VS1_VOSEL	**VOUT selection in binary format**

0620 BUCK_VS1_VOL_CON1 BUCK VS1 VOLTAGE CON1 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VS1_VOSEL						
Type										RW						

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Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VS1_VOSEL	**VOUT selection in SW mode** Voltage = 0.6 + 0.00625 x code

0622 **BUCK_VS1_VOL_CON2** **BUCK VS1 VOLTAGE CON2** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VS1_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VS1_VOSEL_ON	**VOUT selection in normal mode when VOSEL configured in HW mode**

062C **BUCK_VCORE_EN_CON0** **BUCK VCORE ENABLE CON0** **3021**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUCK_VCORE_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	BUCK_VCORE_EN	**Enable control in SW mode**

0630 **BUCK_VCORE_VOL_CON0** **BUCK VCORE VOLTAGE CON0** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DA_NI_VCORE_VOSEL						
Type										RO						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	DA_NI_VCORE_VOSEL	**VOUT selection in binary format**

0632 **BUCK_VCORE_VOL_CON1** **BUCK VCORE VOLTAGE CON1** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VCORE_VOSEL						

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VCORE_VOSEL	**VOUT selection in SW mode** Voltage = 0.6 + 0.00625 x code

0634 BUCK_VCORE_VOL_CON2 BUCK VCORE VOLTAGE CON2 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VCORE_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VCORE_VOSEL_ON	**VOUT selection in normal mode when VOSEL configured in HW mode**

063E BUCK_VCORE2_EN_CON0 BUCK VCORE2 ENABLE CON0 3021

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUCK_VCORE2_EN
Type																RW
Reset																1

Bit(s)	Name	Description
0	BUCK_VCORE2_EN	**Enable control in SW mode**

0642 BUCK_VCORE2_VOL_CON0 BUCK VCORE2 VOLTAGE CON0 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DA_NI_VCORE2_VOSEL						
Type										RO						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	DA_NI_VCORE2_VOSEL	**VOUT selection in binary format**

0644 BUCK_VCORE2_VOL_CON1 BUCK VCORE2 VOLTAGE CON1 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name										BUCK_VCORE2_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VCORE2_VOSEL	**VOUT selection in SW mode** Voltage = 0.6 + 0.00625 x code

0646 BUCK_VCORE2_VOL_CON2 BUCK VCORE2 VOLTAGE CON2 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										BUCK_VCORE2_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	BUCK_VCORE2_VOSEL_ON	**VOUT selection in normal mode when VOSEL configured in HW mode**

064C BUCK_VPA_EN_CON0 BUCK VPA ENABLE CON0 0020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																BUCK_VPA_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	BUCK_VPA_EN	**Enable control in SW mode**

0650 BUCK_VPA_VOL_CON0 BUCK VPA VOLTAGE CON0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DA_NI_VPA_VOSEL					
Type											RO					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	DA_NI_VPA_VOSEL	**VOUT selection in binary format**

0652 BUCK_VPA_VOL_CON1 BUCK VPA VOLTAGE CON1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											BUCK_VPA_VOSEL					

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Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	BUCK_VPA_VOSEL	**VOUT selection in SW mode** Voltage = 0.5 + 0.05 x code

0800 ZCD_CON0 ZCD control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDZCDMUXSEL_VAUDP15				RG_AUDZCDTIMEOUTMODESEL	RG_AUDZCDGAINSTEPSIZE		RG_AUDZCDGAINSTEPTIME			RG_AUDZCDENABLE
Type						RW				RW	RW		RW			RW
Reset						0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
10:8	RG_AUDZCDMUXSEL_VAUDP15	**Zero Crossing Detection mux selection:** 000: LineL and LineR, 001: HPL and HPR, 010: Handset, 011: IV buffer, 100: Bypass ZCD 000: Left line in & Right line in 001: Headphone L & headphone R 010: Handset 011: IV buffer 100: bypass ZCD 101: Bypass ZCD 110: Bypass ZCD 111: Bypass ZCD
6	RG_AUDZCDTIMEOUTMODESEL	
5:4	RG_AUDZCDGAINSTEPSIZE	**Gain Step size to change the internal gain of ZCD.** 00: 1dB. 01: 2dB. 10: 4dB. 11: 8dB.
3:1	RG_AUDZCDGAINSTEPTIME	**Gain Step Time to change the internal gain of ZCD.** 000: 0 us. 001: 250 us 010: 500 us. 011: 1 ms. 100: 2 ms. 101: 4 ms. 110: 8 ms. 111: 16 ms.
0	RG_AUDZCDENABLE	**Enable for zero crossing detection (ZCD) function.** 0: Disable 1: Enable

0802 ZCD_CON1 ZCD control register 1 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDLORGAIN							RG_AUDLOLGAIN				

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Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDLORGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).
4:0	RG_AUDLOLGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).

0804 ZCD_CON2 ZCD control register 2 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDHPRGAIN							RG_AUDHPLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDHPRGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).
4:0	RG_AUDHPLGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).

0806 ZCD_CON3 ZCD control register 3 001F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_AUDHSGAIN				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	RG_AUDHSGAIN	00000: +8dB. 00001: +7dB. 10010: -10dB 11111: -40dB(Mute).

0808 ZCD_CON4 ZCD control register 4 0707

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDIVRGAIN								RG_AUDIVLGAIN		
Type						RW								RW		
Reset						1	1	1						1	1	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
10:8	RG_AUDIVRGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB
2:0	RG_AUDIVLGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB

080A **ZCD_CON5** **ZCD control register 5** **3F3F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDINTGAIN2								RG_AUDINTGAIN1					
Type			RO								RO					
Reset			1	1	1	1	1	1			1	1	1	1	1	1

Bit(s)	Name	Description
13:8	RG_AUDINTGAIN2	
5:0	RG_AUDINTGAIN1	

0A04 **LDO_TOP_CON0** **LDO VA18 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															LDO_VIBR_THER_SDN_EN	
Type															RW	
Reset															0	

Bit(s)	Name	Description
1	LDO_VIBR_THER_SDN_EN	**thermal shout down function enable** 1'b0: disable 1'b1: enable

0A0C **VRTC_CON0** **VRTC control register 0** **8002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VRTC_EN														LDO_VRTC_EN	

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Type	RO														RW	
Reset	1														1	

Bit(s)	Name	Description
15	DA_QI_VRTC_EN	**VRTC enable status**
1	LDO_VRTC_EN	**VRTC enable** 1'b1: enable 1'b0: disable

0A0E **LDO_SHARE_VCN33_CON0** **LDO_SHARE_VCN33_CON0** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LDO_VCN33_EN_SEL_BT													
Type			RW													
Reset			0	1	0											

Bit(s)	Name	Description
13:11	LDO_VCN33_EN_SEL_BT	**VCN33 HW srclk enable selection for BT** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2

0A10 **LDO_SHARE_VCN33_CON1** **LDO_SHARE_VCN33_CON1** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			LDO_VCN33_EN_SEL_WIFI													
Type			RW													
Reset			0	1	0											

Bit(s)	Name	Description
13:11	LDO_VCN33_EN_SEL_WIFI	**VCN33 HW srclk enable selection for WIFI** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2

0A12 **LDO3_VCN33_CON0** **LDO VCN33 control register 0** **0040**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN33_EN	DA_QI_VCN33_STB						DA_QI_VCN33_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VCN33_EN	**VCN33 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VCN33_STB	**VCN33 STB staus**
8	DA_QI_VCN33_MODE	**VCN33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A14 **LDO3_VCN33_OCFB_CON0** **LDO VCN33 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCN33_OCFB_EN	LDO_VCN33_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCN33_OCFB_EN	**VCN33 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VCN33_OCFB_EN	**VCN33 OCFB enable** 1'b1: enable 1'b0: disable

0A1A **LDO1_VLDO28_CON0** **LDO VLDO28 control register 0** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VLDO28_EN	DA_QI_VLDO28_STB						DA_QI_VLDO28_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VLDO28_EN	**VLDO28 enable staus** 1'b1: enable 1'b0: disable

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Bit(s)	Name	Description
14	DA_QI_VLDO28_STB	**VLDO28 STB staus**
8	DA_QI_VLDO28_MODE	**VLDO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A1C **LDO1_VLDO28_OCFB_CON0** **LDO VLDO28 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VLDO28_OCFB_EN	LDO_VLDO28_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VLDO28_OCFB_EN	**VLDO28 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VLDO28_OCFB_EN	**VLDO28 OCFB enable** 1'b1: enable 1'b0: disable

0A24 **LDO_VSRAM_PROC_VOL_CON0** **LDO VSRAM_PROC VOLTAGE CON0** **0050**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										DA_NI_VSRAM_PROC_VOSEL						
Type										RO						
Reset										1	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	DA_NI_VSRAM_PROC_VOSEL	**VOUT selection in binary format**

0A26 **LDO_VSRAM_PROC_VOL_CON1** **LDO VSRAM_PROC VOLTAGE CON1** **0050**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										LDO_VSRAM_PROC_VOSEL						
Type										RW						
Reset										1	0	1	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
6:0	LDO_VSRAM_PROC_VOSEL	**VOUT selection in SW mode** Voltage = 0.6 + 0.00625 x code

0A28 **LDO_VSRAM_PROC_VOL_CON2** **LDO VSRAM_PROC VOLTAGE CON2** **0050**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										LDO_VSRAM_PROC_VOSEL_ON						
Type										RW						
Reset										1	0	1	0	0	0	0

Bit(s)	Name	Description
6:0	LDO_VSRAM_PROC_VOSEL_ON	**VOUT selection in normal mode when VOSEL configured in HW mode**

0A2E **LDO_BATON_CON0** **LDO_BATON_CON0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												LDO_BATON_HT_EN_DLY_TIME				LDO_BATON_HT_EN
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
4	LDO_BATON_HT_EN_DLY_TIME	**BATON high-temperature detection delay time** 1'b0: 6T 1'b1: 12T
0	LDO_BATON_HT_EN	**Battery-On HW high temperature detection** 1'b0: disable 1'b1: enable

0A30 **LDO2_TREF_CON0** **LDO TREF control register 0** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_TREF_EN		LDO_TREF_EN_SEL													
Type	RO		RW													
Reset	0		0	1	0											

Bit(s)	Name	Description
15	DA_QI_TREF_EN	**TREF enable staus**

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Bit(s)	Name	Description
		1'b1: enable 1'b0: disable
13:11	LDO_TREF_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2

0A32 **LDO3_VTCXO28_CON0** **LDO VTCXO28 control register 0** **1040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VTCXO28_EN	DA_QI_VTCXO28_STB	LDO_VTCXO28_EN_SEL					DA_QI_VTCXO28_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VTCXO28_EN	**VTCXO28 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VTCXO28_STB	**VTCXO28 STB staus**
13:11	LDO_VTCXO28_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VTCXO28_MODE	**VTCXO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A34 **LDO3_VTCXO28_OCFB_CON0** **LDO VTCXO28 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VTCXO28_OCFB_EN	LDO_VTCXO28_OCFB_EN									
Type						RO	RW									

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Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VTCXO28_OCFB_EN	**VTCXO28 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VTCXO28_OCFB_EN	**VTCXO28 OCFB enable** 1'b1: enable 1'b0: disable

0A36 LDO3_VTCXO24_CON0 LDO VTCXO24 control register 0 1042

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VTCXO24_EN	DA_QI_VTCXO24_STB	LDO_VTCXO24_EN_SEL					DA_QI_VTCXO24_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VTCXO24_EN	**VTCXO24 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VTCXO24_STB	**VTCXO24 STB staus**
13:11	LDO_VTCXO24_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VTCXO24_MODE	**VTCXO24 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A38 LDO3_VTCXO24_OCFB_CON0 LDO VTCXO24 control register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VTCXO24_OCFB_EN	LDO_VTCXO24_OCFB_EN									
Type						RO	RW									
Reset						0	0									

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Bit(s)	Name	Description
10	DA_QI_VTCXO24_OCFB_EN	**VTCXO24 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VTCXO24_OCFB_EN	**VTCXO24 OCFB enable** 1'b1: enable 1'b0: disable

0A3A LDO3_VXO22_CON0 LDO VXO22 control register 0 1042

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VXO22_EN	DA_QI_VXO22_STB	LDO_VXO22_EN_SEL					DA_QI_VXO22_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VXO22_EN	**VXO22 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VXO22_STB	**VXO22 STB staus**
13:11	LDO_VXO22_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VXO22_MODE	**VXO22 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A3C LDO3_VXO22_OCFB_CON0 LDO VXO22 control register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VXO22_OCFB_EN	LDO_VXO22_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VXO22_OCF	**VXO22 OCFB status**

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Bit(s)	Name	Description
	B_EN	1'b1: over current occur 1'b0: no over current occur
9	LDO_VXO22_OCFB_EN	**VXO22 OCFB enable** 1'b1: enable 1'b0: disable

0A3E **LDO3_VRF18_CON0** **LDO VRF18 control register 0** **1040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VRF18_EN**	**DA_QI_VRF18_STB**	**LDO_VRF18_EN_SEL**					**DA_QI_VRF18_MODE**								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VRF18_EN	**VRF18 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VRF18_STB	**VRF18 STB staus**
13:11	LDO_VRF18_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VRF18_MODE	**VRF18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A40 **LDO3_VRF18_OCFB_CON0** **LDO VRF18 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VRF18_OCFB_EN**	**LDO_VRF18_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VRF18_OCFB_EN	**VRF18 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VRF18_OCFB_	**VRF18 OCFB enable**

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Bit(s)	Name	Description
	EN	1'b1: enable 1'b0: disable

0A42 **LDO3_VRF12_CON0** **LDO VRF12 control register 0** **1040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VRF12_EN	DA_QI_VRF12_STB	LDO_VRF12_EN_SEL					DA_QI_VRF12_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VRF12_EN	**VRF12 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VRF12_STB	**VRF12 STB staus**
13:11	LDO_VRF12_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VRF12_MODE	**VRF12 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A44 **LDO3_VRF12_OCFB_CON0** **LDO VRF12 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VRF12_OCFB_EN	LDO_VRF12_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VRF12_OCFB_EN	**VRF12 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VRF12_OCFB_EN	**VRF12 OCFB enable** 1'b1: enable 1'b0: disable

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0A48 **LDO3_VCN28_CON0** **LDO VCN28 control register 0** **1040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN28_EN	DA_QI_VCN28_STB	LDO_VCN28_EN_SEL					DA_QI_VCN28_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VCN28_EN	**VCN28 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VCN28_STB	**VCN28 STB staus**
13:11	LDO_VCN28_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VCN28_MODE	**VCN28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A4A **LDO3_VCN28_OCFB_CON0** **LDO VCN28 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCN28_OCFB_EN	LDO_VCN28_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCN28_OCFB_EN	**VCN28 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VCN28_OCFB_EN	**VCN28 OCFB enable** 1'b1: enable 1'b0: disable

0A4C **LDO3_VCN18_CON0** **LDO VCN18 control register 0** **1040**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN18_EN	DA_QI_VCN18_STB	LDO_VCN18_EN_SEL					DA_QI_VCN18_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VCN18_EN	**VCN18 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VCN18_STB	**VCN18 STB staus**
13:11	LDO_VCN18_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VCN18_MODE	**VCN18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A4E LDO3_VCN18_OCFB_CON0 LDO VCN18 control register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCN18_OCFB_EN	LDO_VCN18_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCN18_OCFB_EN	**VCN18 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VCN18_OCFB_EN	**VCN18 OCFB enable** 1'b1: enable 1'b0: disable

0A50 LDO0_VCAMA_CON0 LDO VCAMA control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMA_EN	DA_QI_VCAMA_STB						DA_QI_VCAMA_MO								

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								DE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VCAMA_EN	**VCAMA enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VCAMA_STB	**VCAMA STB staus**
8	DA_QI_VCAMA_MODE	**VCAMA low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A52 **LDO0_VCAMA_OCFB_CON0** **LDO VCAMA control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCAMA_OCFB_EN	LDO_VCAMA_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCAMA_OCFB_EN	**VCAMA OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VCAMA_OCFB_EN	**VCAMA OCFB enable** 1'b1: enable 1'b0: disable

0A54 **LDO0_VCAMIO_CON0** **LDO VCAMIO control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMIO_EN	DA_QI_VCAMIO_STB						DA_QI_VCAMIO_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VCAMIO_EN	**VCAMIO enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VCAMIO_STB	**VCAMIO STB staus**
8	DA_QI_VCAMIO_MODE	**VCAMIO low power mode status** 1'b0: Normal mode

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Bit(s)	Name	Description
		1'b1: Low power mode

0A56 **LDO0_VCAMIO_OCFB_CON0** **LDO VCAMIO control register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VCAMIO_OCFB_EN	LDO_VCAMIO_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCAMIO_OCFB_EN	**VCAMIO OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VCAMIO_OCFB_EN	**VCAMIO OCFB enable** 1'b1: enable 1'b0: disable

0A58 **LDO0_VCAMD_CON0** **LDO VCAMD control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMD_EN	DA_QI_VCAMD_STB						DA_QI_VCAMD_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VCAMD_EN	**VCAMD enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VCAMD_STB	**VCAMD STB staus**
8	DA_QI_VCAMD_MODE	**VCAMD low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A5A **LDO0_VCAMD_OCFB_CON0** **LDO VCAMD control register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VC	LDO_VCA									

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						AMD_OCFB_EN	MD_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VCAMD_OCFB_EN	**VCAMD OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VCAMD_OCFB_EN	**VCAMD OCFB enable** 1'b1: enable 1'b0: disable

0A5C **LDO3_VAUX18_CON0** LDO VAUX18 control register 0 1042

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VAUX18_EN	DA_QI_VAUX18_STB	LDO_VAUX18_EN_SEL					DA_QI_VAUX18_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VAUX18_EN	**VAUX18 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VAUX18_STB	**VAUX18 STB staus**
13:11	LDO_VAUX18_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VAUX18_MODE	**VAUX18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A5E **LDO3_VAUX18_OCFB_CON0** LDO VAUX18 control register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VAUX18_OCFB_EN	LDO_VAUX18_OCFB_EN									
Type						RO	RW									

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Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VAUX18_OCFB_EN	**VAUX18 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VAUX18_OCFB_EN	**VAUX18 OCFB enable** 1'b1: enable 1'b0: disable

0A60 LDO3_VAUD28_CON0 LDO VAUD28 control register 0 1042

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VAUD28_EN	DA_QI_VAUD28_STB	LDO_VAUD28_EN_SEL					DA_QI_VAUD28_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VAUD28_EN	**VAUD28 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VAUD28_STB	**VAUD28 STB staus**
13:11	LDO_VAUD28_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VAUD28_MODE	**VAUD28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A62 LDO3_VAUD28_OCFB_CON0 LDO VAUD28 control register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VAUD28_OCFB_EN	LDO_VAUD28_OCFB_EN									
Type						RO	RW									
Reset						0	0									

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Bit(s)	Name	Description
10	DA_QI_VAUD28_OCFB_EN	**VAUD28 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VAUD28_OCFB_EN	**VAUD28 OCFB enable** 1'b1: enable 1'b0: disable

0A64 **LDO3_VSRAM_PROC_CON0** **LDO VSRAM_PROC control register 0** **1042**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VSRAM_PROC_EN	DA_QI_VSRAM_PROC_STB	LDO_VSRAM_PROC_EN_SEL					DA_QI_VSRAM_PROC_MODE								
Type	RO	RO	RW					RO								
Reset	0	0	0	1	0			0								

Bit(s)	Name	Description
15	DA_QI_VSRAM_PROC_EN	**VSRAM_PROC enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VSRAM_PROC_STB	**VSRAM_PROC STB staus**
13:11	LDO_VSRAM_PROC_EN_SEL	**HW srclk enable selection** 3'b000: SRCLKEN_IN0 3'b001: SRCLKEN_IN1 3'b010: SRCLKEN_IN0 | SRCLKEN_IN1 3'b011: SRCLKEN_IN0 & SRCLKEN_IN1 3'b100: SRCLKEN_IN2 3'b101: SRCLKEN_IN0 | SRCLKEN_IN2 3'b110: SRCLKEN_IN1 | SRCLKEN_IN2 3'b111: SRCLKEN_IN0 | SRCLKEN_IN1 | SRCLKEN_IN2
8	DA_QI_VSRAM_PROC_MODE	**VSRAM_PROC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A66 **LDO3_VSRAM_PROC_OCFB_CON0** **LDO VSRAM_PROC control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VSRAM_PROC_OCFB_EN	LDO_VSRAM_PROC_OCFB_EN									
Type						RO	RW									
Reset						0	0									

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Bit(s)	Name	Description
10	DA_QI_VSRAM_PROC_OCFB_EN	**VSRAM_PROC OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VSRAM_PROC_OCFB_EN	**VSRAM_PROC OCFB enable** 1'b1: enable 1'b0: disable

0A68 **LDO1_VDRAM_CON0** **LDO VDRAM control register 0** **0042**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VDRAM_EN**	**DA_QI_VDRAM_STB**						**DA_QI_VDRAM_MODE**								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VDRAM_EN	**VDRAM enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VDRAM_STB	**VDRAM STB staus**
8	DA_QI_VDRAM_MODE	**VDRAM low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A6A **LDO1_VDRAM_OCFB_CON0** **LDO VDRAM control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VDRAM_OCFB_EN**	**LDO_VDRAM_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VDRAM_OCFB_EN	**VDRAM OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VDRAM_OCFB_EN	**VDRAM OCFB enable** 1'b1: enable 1'b0: disable

0A6E **LDO1_VSIM1_** **LDO VSIM1 control register 0** **0040**

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CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VSIM1_EN	DA_QI_VSIM1_STB						DA_QI_VSIM1_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VSIM1_EN	**VSIM1 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VSIM1_STB	**VSIM1 STB staus**
8	DA_QI_VSIM1_MODE	**VSIM1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A70 **LDO1_VSIM1_OCFB_CON0** **LDO VSIM1 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VSIM1_OCFB_EN	LDO_VSIM1_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VSIM1_OCFB_EN	**VSIM1 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VSIM1_OCFB_EN	**VSIM1 OCFB enable** 1'b1: enable 1'b0: disable

0A72 **LDO1_VSIM2_CON0** **LDO VSIM2 control register 0** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VSIM2_EN	DA_QI_VSIM2_STB						DA_QI_VSIM2_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VSIM2_EN	**VSIM2 enable staus** 1'b1: enable

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Bit(s)	Name	Description
		1'b0: disable
14	DA_QI_VSIM2_STB	**VSIM2 STB staus**
8	DA_QI_VSIM2_MODE	**VSIM2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A74 **LDO1_VSIM2_OCFB_CON0** **LDO VSIM2 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VSIM2_OCFB_EN**	**LDO_VSIM2_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VSIM2_OCFB_EN	**VSIM2 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VSIM2_OCFB_EN	**VSIM2 OCFB enable** 1'b1: enable 1'b0: disable

0A76 **LDO1_VIO28_CON0** **LDO VIO28 control register 0** **0042**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VIO28_EN**	**DA_QI_VIO28_STB**						**DA_QI_VIO28_MODE**								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VIO28_EN	**VIO28 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VIO28_STB	**VIO28 STB staus**
8	DA_QI_VIO28_MODE	**VIO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A78 **LDO1_VIO28_OCFB_CON0** **LDO VIO28 control register 1** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VIO28_OCFB_EN	LDO_VIO28_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VIO28_OCFB_EN	**VIO28 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VIO28_OCFB_EN	**VIO28 OCFB enable** 1'b1: enable 1'b0: disable

0A7A **LDO1_VMC_CON0** **LDO VMC control register 0** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VMC_EN	DA_QI_VMC_STB						DA_QI_VMC_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VMC_EN	**VMC enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VMC_STB	**VMC STB staus**
8	DA_QI_VMC_MODE	**VMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A7C **LDO1_VMC_OCFB_CON0** **LDO VMC control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VMC_OCFB_EN	LDO_VMC_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VMC_OCFB_EN	**VMC OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VMC_OCFB_E	**VMC OCFB enable**

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Bit(s)	Name	Description
	N	1'b1: enable 1'b0: disable

0A80 **LDO1_VMCH_CON0** **LDO VMCH control register 0** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VMCH_EN	DA_QI_VMCH_STB						DA_QI_VMCH_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VMCH_EN	**VMCH enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VMCH_STB	**VMCH STB staus**
8	DA_QI_VMCH_MODE	**VMCH low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A82 **LDO1_VMCH_OCFB_CON0** **LDO VMCH control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VMCH_OCFB_EN	LDO_VMCH_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VMCH_OCFB_EN	**VMCH OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VMCH_OCFB_EN	**VMCH OCFB enable** 1'b1: enable 1'b0: disable

0A86 **LDO1_VUSB33_CON0** **LDO VUSB33 control register 0** **0042**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VUSB33_EN	DA_QI_VUSB33_STB						DA_QI_VUSB33_MO								

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VUSB33_EN	**VUSB33 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VUSB33_STB	**VUSB33 STB staus**
8	DA_QI_VUSB33_MODE	**VUSB33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A88 **LDO1_VUSB33_OCFB_CON0** **LDO VUSB33 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**DA_QI_VUSB33_OCFB_EN**	**LDO_VUSB33_OCFB_EN**									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VUSB33_OCFB_EN	**VUSB33 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VUSB33_OCFB_EN	**VUSB33 OCFB enable** 1'b1: enable 1'b0: disable

0A8A **LDO1_VEMC33_CON0** **LDO VEMC33 control register 0** **0242**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VEMC33_EN**	**DA_QI_VEMC33_STB**						**DA_QI_VEMC33_MODE**								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VEMC33_EN	**VEMC33 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VEMC33_STB	**VEMC33 STB staus**
8	DA_QI_VEMC33_MODE	**VEMC33 low power mode status** 1'b0: Normal mode

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Bit(s)	Name	Description
		1'b1: Low power mode

0A8C **LDO1_VEMC33_OCFB_CON0** **LDO VEMC33 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VEMC33_OCFB_EN	LDO_VEMC33_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VEMC33_OCFB_EN	**VEMC33 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VEMC33_OCFB_EN	**VEMC33 OCFB enable** 1'b1: enable 1'b0: disable

0A90 **LDO1_VIO18_CON0** **LDO VIO18 control register 0** **0042**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VIO18_EN	DA_QI_VIO18_STB						DA_QI_VIO18_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VIO18_EN	**VIO18 enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VIO18_STB	**VIO18 STB staus**
8	DA_QI_VIO18_MODE	**VIO18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A92 **LDO1_VIO18_OCFB_CON0** **LDO VIO18 control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VIO18_	LDO_VIO18_OC									

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						OCFB_EN	FB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VIO18_OCFB_EN	**VIO18 OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VIO18_OCFB_EN	**VIO18 OCFB enable** 1'b1: enable 1'b0: disable

0A94 **LDO0_VIBR_CON0** **LDO VIBR control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VIBR_EN	DA_QI_VIBR_STB						DA_QI_VIBR_MODE								
Type	RO	RO						RO								
Reset	0	0						0								

Bit(s)	Name	Description
15	DA_QI_VIBR_EN	**VIBR enable staus** 1'b1: enable 1'b0: disable
14	DA_QI_VIBR_STB	**VIBR STB staus**
8	DA_QI_VIBR_MODE	**VIBR low power mode status** 1'b0: Normal mode 1'b1: Low power mode

0A96 **LDO0_VIBR_OCFB_CON0** **LDO VIBR control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DA_QI_VIBR_OCFB_EN	LDO_VIBR_OCFB_EN									
Type						RO	RW									
Reset						0	0									

Bit(s)	Name	Description
10	DA_QI_VIBR_OCFB_EN	**VIBR OCFB status** 1'b1: over current occur 1'b0: no over current occur
9	LDO_VIBR_OCFB_EN	**VIBR OCFB enable** 1'b1: enable 1'b0: disable

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0A98 **ALDO_ANA_CON0** **ALDO control register 0** **1300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VTCXO28_NDIS_EN			RG_VTCXO28_VOSEL						RG_VTCXO28_CAL			
Type				RW			RW						RW			
Reset				1			1	1					0	0	0	0

Bit(s)	Name	Description
12	RG_VTCXO28_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
9:8	RG_VTCXO28_VOSEL	**2'b00: 1.8V** 2'b01: 2.2V 2'b10: 2.375V 2'b11: 2.8V
3:0	RG_VTCXO28_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0A9A **ALDO_ANA_CON1** **ALDO control register 1** **1300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VAUD28_NDIS_EN			RG_VAUD28_VOSEL						RG_VAUD28_CAL			
Type				RW			RW						RW			
Reset				1			1	1					0	0	0	0

Bit(s)	Name	Description
12	RG_VAUD28_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
9:8	RG_VAUD28_VOSEL	**2'b00: 1.8V**

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Bit(s)	Name	Description
		2'b01: 2.2V 2'b10: 2.375V 2'b11: 2.8V
3:0	RG_VAUD28_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0A9C **ALDO_ANA_CON2** **ALDO control register 2** **1300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_VCN28_NDIS_EN**			**RG_VCN28_VOSEL**						**RG_VCN28_CAL**			
Type				RW			RW						RW			
Reset				1			1	1					0	0	0	0

Bit(s)	Name	Description
12	RG_VCN28_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
9:8	RG_VCN28_VOSEL	**2'b00: 1.8V** 2'b01: 2.2V 2'b10: 2.375V 2'b11: 2.8V
3:0	RG_VCN28_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV

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Bit(s)	Name	Description
		4'b1110: +40 mV 4'b1111: +20 mV

0A9E **ALDO_ANA_CON3** **ALDO control register 3** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VAUX18_NDIS_EN			RG_VAUX18_VOSEL						RG_VAUX18_CAL			
Type				RW			RW						RW			
Reset				1			0	0					0	0	0	0

Bit(s)	Name	Description
12	RG_VAUX18_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
9:8	RG_VAUX18_VOSEL	**2'b00: 1.8V** 2'b01: 2.2V 2'b10: 2.375V 2'b11: 2.8V
3:0	RG_VAUX18_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0AA0 **ALDO_ANA_CON4** **ALDO control register 4** **1300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCAMA_NDIS_EN			RG_VCAMA_VOSEL						RG_VCAMA_CAL			
Type				RW			RW						RW			
Reset				1			1	1					0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
12	RG_VCAMA_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
9:8	RG_VCAMA_VOSEL	**voltage selection** 2b'10: 2.5V 2b'11: 2.8V
3:0	RG_VCAMA_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0AA2 **ALDO_ANA_CON5** **ALDO control register 5** **03FF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_ALDO_RSV_H									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
9:0	RG_ALDO_RSV_H	**Reserve level shift(default High)**

0AA4 **ALDO_ANA_CON6** **ALDO control register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_ALDO_RSV_L									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	RG_ALDO_RSV_L	**Reserve level shift(default Low)**

0AA6 **DLDO_ANA_CON0** **DLDO control register 0** **1100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name				**RG_VXO22_NDIS_EN**			**RG_VXO22_VOSEL**						**RG_VXO22_CAL**			
Type				RW			RW						RW			
Reset				1			0	1					0	0	0	0

Bit(s)	Name	Description
12	RG_VXO22_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
9:8	RG_VXO22_VOSEL	**2'b00: 1.8V** 2'b01: 2.2V 2'b10: 2.375V 2'b11: 2.8V
3:0	RG_VXO22_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0AA8 **DLDO_ANA_CON1** **DLDO control register 1** **1200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_VTCXO24_NDIS_EN**			**RG_VTCXO24_VOSEL**						**RG_VTCXO24_CAL**			
Type				RW			RW						RW			
Reset				1			1	0					0	0	0	0

Bit(s)	Name	Description
12	RG_VTCXO24_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
9:8	RG_VTCXO24_VOSEL	**2'b00: 1.8V** 2'b01: 2.2V 2'b10: 2.375V 2'b11: 2.8V
3:0	RG_VTCXO24_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV

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Bit(s)	Name	Description
		4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0AAA **DLDO_ANA_CON2** **DLDO control register 2** **1200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_VSIM1_NDIS_EN**		**RG_VSIM1_VOSEL**							**RG_VSIM1_CAL**			
Type				RW		RW							RW			
Reset				1		0	1	0					0	0	0	0

Bit(s)	Name	Description
12	RG_VSIM1_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
10:8	RG_VSIM1_VOSEL	**output selection signal** 3'b000: not use 3'b001: 1.7 V 3'b010: 1.8 V 3'b011: 1.86 V 3'b101: 2.76V 3'b110: 3.0 V 3'b111: 3.1 V
3:0	RG_VSIM1_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

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0AAC **DLDO_ANA_CON3** **DLDO control register 3** **1200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VSIM2_NDIS_EN		RG_VSIM2_VOSEL							RG_VSIM2_CAL			
Type				RW		RW							RW			
Reset				1		0	1	0					0	0	0	0

Bit(s)	Name	Description
12	RG_VSIM2_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
10:8	RG_VSIM2_VOSEL	**output selection signal** 3'b000: not use 3'b001: 1.7 V 3'b010: 1.8 V 3'b011: 1.86 V 3'b101: 2.76V 3'b110: 3.0 V 3'b111: 3.1 V
3:0	RG_VSIM2_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0AAE **DLDO_ANA_CON4** **DLDO control register 4** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCN33_NDIS_EN		RG_VCN33_VOSEL							RG_VCN33_CAL			
Type				RW		RW							RW			
Reset				1		0	0	0					0	0	0	0

Bit(s)	Name	Description
12	RG_VCN33_NDIS_E	**LDO output power down Enable**

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Bit(s)	Name	Description
	N	1'b0: disable output powerdown 1'b1: enable output powerdown
10:8	RG_VCN33_VOSEL	**Output Voltage Selection** (2'b00: 3.3 v) 3'b000: 3.3 v 3'b001: 3.4 v 3'b010: 3.5 v 3'b011: 3.6 v 3'b1xx: no use
3:0	RG_VCN33_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0AB0 **DLDO_ANA_CON5** **DLDO control register 5** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_VUSB33_NDIS_EN**									**RG_VUSB33_CAL**			
Type				RW									RW			
Reset				1									0	0	0	0

Bit(s)	Name	Description
12	RG_VUSB33_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
3:0	RG_VUSB33_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV

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Bit(s)	Name	Description
		4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0AB2 **DLDO_ANA_CON6** **DLDO control register 6** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VMCH_NDIS_EN			RG_VMCH_VOSEL						RG_VMCH_CAL			
Type				RW			RW						RW			
Reset				1			0	0					0	0	0	0

Bit(s)	Name	Description
12	RG_VMCH_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
9:8	RG_VMCH_VOSEL	**Output Voltage Selection** (2'b00: 2.9 v) 2'b00: 2.9 v 2'b01: 3.0 v 2'b10: 3.3 v 2'b11: not use
3:0	RG_VMCH_CAL	**Voltage Calibration** (4'b0000: 0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0AB4 **DLDO_ANA_CON7** **DLDO control register 7** **0500**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VMCH_STB_SEL	RG_VMCH_CL_EN	RG_VMCH_DL_EN	RG_VMCH_DUMMY_LOAD				RG_VMCH_OC_TRIM			
Type						RW	RW	RW	RW				RW			
Reset						1	0	1	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
10	RG_VMCH_STB_SEL	**Soft start time select** 1'b0:100~240usec 1'b1:40usec
9	RG_VMCH_CL_EN	**Constant load control** (1'b1: enable; 1'b0: disable)
8	RG_VMCH_DL_EN	**Dynamic load control** (1'b1: enable; 1'b0: disable)
7:4	RG_VMCH_DUMMY_LOAD	**Dummy load**
3:0	RG_VMCH_OC_TRIM	**OC trimming**

0AB6 **DLDO_ANA_CON8** **DLDO control register 8** **1100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VEMC33_NDIS_EN			RG_VEMC33_VOSEL						RG_VEMC33_CAL			
Type				RW			RW						RW			
Reset				1			0	1					0	0	0	0

Bit(s)	Name	Description
12	RG_VEMC33_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
9:8	RG_VEMC33_VOSEL	**Output Voltage Selection** (2'b00: 2.9 v) 2'b00: 2.9 v 2'b01: 3.0 v 2'b10: 3.3 v 2'b11: not use
3:0	RG_VEMC33_CAL	**Voltage Calibration** (4'b0000: 0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

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0AB8 **DLDO_ANA_CON9** **DLDO control register 9** **03F0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VEMC33_STB_SEL	RG_VEMC33_CL_EN	RG_VEMC33_DL_EN	RG_VEMC33_DUMMY_LOAD				RG_VEMC33_OC_TRIM			
Type						RW	RW	RW	RW				RW			
Reset						0	1	1	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
10	RG_VEMC33_STB_SEL	**Soft start time select** 1'b0:100~240usec 1'b1:40usec
9	RG_VEMC33_CL_EN	**Constant load control** (1'b1: enable; 1'b0: disable)
8	RG_VEMC33_DL_EN	**Dynamic load control** (1'b1: enable; 1'b0: disable)
7:4	RG_VEMC33_DUMMY_LOAD	**Dummy load**
3:0	RG_VEMC33_OC_TRIM	**OC trimming**

0ABA **DLDO_ANA_CON10** **DLDO control register 10** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VIO28_NDIS_EN									RG_VIO28_CAL			
Type				RW									RW			
Reset				1									0	0	0	0

Bit(s)	Name	Description
12	RG_VIO28_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
3:0	RG_VIO28_CAL	**Voltage Calibration** (4'b0000:0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV

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Bit(s)	Name	Description
		4'b1111: 20 mV

0ABC **DLDO_ANA_CON11** **DLDO control register 11** **1500**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VIBR_NDIS_EN		RG_VIBR_VOSEL							RG_VIBR_CAL			
Type				RW		RW							RW			
Reset				1		1	0	1					0	0	0	0

Bit(s)	Name	Description
12	RG_VIBR_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
10:8	RG_VIBR_VOSEL	**Output Voltage Selection** (3'b101: 2.8 v) 3'b000: 1.2 v 3'b001: 1.3 v 3'b010: 1.5 v 3'b011: 1.8 v 3'b100: 2.5 v 3'b101: 2.8 v 3'b110: 3.0 v 3'b111: 3.3 v
3:0	RG_VIBR_CAL	**Voltage Calibration** (4'b0000:0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0ABE **DLDO_ANA_CON12** **DLDO control register 12** **1500**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VLDO28_NDIS_EN		RG_VLDO28_VOSEL							RG_VLDO28_CAL			
Type				RW		RW							RW			
Reset				1		1	0	1					0	0	0	0

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Bit(s)	Name	Description
12	RG_VLDO28_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
10:8	RG_VLDO28_VOSEL	**Output Voltage Selection** (3'b101: 2.8 v) 3'b000: 1.2 v 3'b001: 1.3 v 3'b010: 1.5 v 3'b011: 1.8 v 3'b100: 2.5 v 3'b101: 2.8 v 3'b110: 3.0 v 3'b111: 3.3 v
3:0	RG_VLDO28_CAL	**Voltage Calibration** (4'b0000:0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0AC0 **DLDO_ANA_CON13** **DLDO control register 13** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_VLDO28_CL_EN	RG_VLDO28_DL_EN	RG_VLDO28_DUMMY_LOAD			
Type											RW	RW	RW			
Reset											0	1	0	0	0	0

Bit(s)	Name	Description
5	RG_VLDO28_CL_EN	**Constant load control** (1'b1: enable; 1'b0: disable)
4	RG_VLDO28_DL_EN	**Dynamic load control** (1'b1: enable; 1'b0: disable)
3:0	RG_VLDO28_DUMMY_LOAD	**Dummy load**

0AC2 **DLDO_ANA_C** **DLDO control register 14** **2500**

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ON14

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VMC_NDIS_EN			RG_VMC_VOSEL							RG_VMC_CAL			
Type			RW			RW							RW			
Reset			1			1	0	1					0	0	0	0

Bit(s)	Name	Description
13	RG_VMC_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
10:8	RG_VMC_VOSEL	**3'b000: 1.2 v** 3'b001: 1.3 v 3'b010: 1.5 v 3'b011: 1.8 v 3'b100: 2.5 v 3'b101: 2.9 v (Normal) 3'b110: 3.0 v 3'b111: 3.3 v
3:0	RG_VMC_CAL	**Voltage Calibration** (4'b0000:0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0AC4 **DLDO_ANA_CON15** **DLDO control register 15** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_VMC_CL_EN	RG_VMC_DL_EN	RG_VMC_DUMMY_LOAD			
Type											RW	RW	RW			
Reset											0	1	0	0	0	0

Bit(s)	Name	Description
5	RG_VMC_CL_EN	**Constant load control** (1'b1: enable; 1'b0: disable)
4	RG_VMC_DL_EN	**Dynamic load control** (1'b1: enable; 1'b0: disable)
3:0	RG_VMC_DUMMY_L	**Dummy load**

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Bit(s)	Name	Description
	OAD	

0AC6 **DLDO_ANA_CON16** **DLDO control register 16** **03FF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DLDO_RSV_H									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
9:0	RG_DLDO_RSV_H	**Reserve level shift(default High)**

0AC8 **DLDO_ANA_CON17** **DLDO control register 17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DLDO_RSV_L									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	RG_DLDO_RSV_L	**Reserve level shift(default Low)**

0ACA **SLDO_ANA_CON0** **SLDO control register 0** **1400**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCAMD_NDIS_EN		RG_VCAMD_VOSEL							RG_VCAMD_CAL			
Type				RW		RW							RW			
Reset				1		1	0	0					0	0	0	0

Bit(s)	Name	Description
12	RG_VCAMD_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
10:8	RG_VCAMD_VOSEL	**Output Voltage Selection** (3'b100: 1.3 v) 3'b000: 0.9 v 3'b001: 1.0 v 3'b010: 1.1 v 3'b011: 1.22 v 3'b100: 1.3 v 3'b101: 1.5 v 3'b110: 1.8 v
3:0	RG_VCAMD_CAL	**Voltage Calibration** (4'b0000:0mV)

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Bit(s)	Name	Description
		4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0ACC **SLDO_ANA_CON1** **SLDO control register 1** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VRF18_NDIS_EN									RG_VRF18_CAL			
Type				RW									RW			
Reset				1									0	0	0	0

Bit(s)	Name	Description
12	RG_VRF18_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
3:0	RG_VRF18_CAL	**Voltage Calibration** (4'b0000:0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0ACE **SLDO_ANA_CON2** **SLDO control register 2** **1400**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VRF12	RG_VRF12		RG_VRF12_VOSEL							RG_VRF12_CAL			

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			_STB_SEL	_NDIS_EN												
Type			RW	RW		RW							RW			
Reset			0	1		1	0	0					0	0	0	0

Bit(s)	Name	Description
13	RG_VRF12_STB_SEL	**LDO Softstart function Enable** 1'b0: enable softstart function 1'b1: disable softstart function
12	RG_VRF12_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
10:8	RG_VRF12_VOSEL	**output selection signal** (3'b111 : 1.8 V) 3'b000 : 0.9V 3'b001 : 0.95V 3'b010 : 0.1V 3'b011 : 1.05V 3'b100 : 1.2V 3'b101 : 1.5V 3'b110 : 1.8V 3'b111 : no use
3:0	RG_VRF12_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -10 mV 4'b0010: -20 mV 4'b0011: -30 mV 4'b0100: -40 mV 4'b0101: -50 mV 4'b0110: -60 mV 4'b0111: -70 mV 4'b1000: +10 mV 4'b1001: +20 mV 4'b1010: +30 mV 4'b1011: +40 mV 4'b1100: +50 mV 4'b1101: +60 mV 4'b1110: +70 mV 4'b1111: +80 mV

0AD0 **SLDO_ANA_CON3** **SLDO control register 3** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_VRF12_CL_EN	RG_VRF12_DL_EN	RG_VRF12_DUMMY_LOAD				
Type										RW	RW	RW				
Reset										0	1	0	0	0	0	0

Bit(s)	Name	Description
6	RG_VRF12_CL_EN	**Constant load control** (1'b1: enable; 1'b0: disable)
5	RG_VRF12_DL_EN	**Dynamic load control**

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Bit(s)	Name	Description
		(1'b1: enable; 1'b0: disable)
4:0	RG_VRF12_DUMMY_LOAD	**dumy load option:** 00000:0mA 00001:vo/200 mA 00010:vo/400 mA 00100:vo/800 mA 01000:vo/1600 mA 10000:vo/3200 mA

0AD2 SLDO_ANA_CON4 SLDO control register 4 1000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VIO18_NDIS_EN									RG_VIO18_CAL			
Type				RW									RW			
Reset				1									0	0	0	0

Bit(s)	Name	Description
12	RG_VIO18_NDIS_EN	**LDO output power down Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
3:0	RG_VIO18_CAL	**LDO Voltage Calibration** (4'b0000:0 mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: +160 mV 4'b1001: +140 mV 4'b1010: +120 mV 4'b1011: +100 mV 4'b1100: +80 mV 4'b1101: +60 mV 4'b1110: +40 mV 4'b1111: +20 mV

0AD4 SLDO_ANA_CON5 SLDO control register 5 4800

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VDRAM_CL_EN	RG_VDRAM_DL_EN	RG_VDRAM_PCUR_CAL		RG_VDRAM_NDIS_EN		RG_VDRAM_VOSEL						RG_VDRAM_CAL			
Type	RW	RW	RW		RW		RW						RW			
Reset	0	1	0	0	1		0	0					0	0	0	0

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Bit(s)	Name	Description
15	RG_VDRAM_CL_EN	**Constant load control** (1'b1: enable; 1'b0: disable)
14	RG_VDRAM_DL_EN	**Dynamic load control** (1'b1: enable; 1'b0: disable)
13:12	RG_VDRAM_PCUR_CAL	**Pulse current calibration**
11	RG_VDRAM_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
9:8	RG_VDRAM_VOSEL	**Output Voltage Selection** 2'b00: 1.24 v 2'b01: 1.39 v 2'b10: 1.54 v 2'b11: 1.54 v
3:0	RG_VDRAM_CAL	**Voltage Calibration** (4'b0000:0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0AD6 **SLDO_ANA_CON6** **SLDO control register 6** **1300**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCAMIO_NDIS_EN			RG_VCAMIO_VOSEL						RG_VCAMIO_CAL			
Type				RW			RW						RW			
Reset				1			1	1					0	0	0	0

Bit(s)	Name	Description
12	RG_VCAMIO_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
9:8	RG_VCAMIO_VOSEL	**Output Voltage Selection** (2'b11: 1.8 v) 2'b00: 1.2 v 2'b01: 1.3 v 2'b10: 1.5 v 2'b11: 1.8 v
3:0	RG_VCAMIO_CAL	**Voltage Calib+F30ration** (4'b0000:0mV)

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Bit(s)	Name	Description
		4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0AD8 **SLDO_ANA_CON7** **SLDO control register 7** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCN18_NDIS_EN									RG_VCN18_CAL			
Type				RW									RW			
Reset				1									0	0	0	0

Bit(s)	Name	Description
12	RG_VCN18_NDIS_EN	**POWER DOWN NMOS Enable** (1'b1: enable; 1'b0: disable)
3:0	RG_VCN18_CAL	**Voltage Calibration** (4'b0000:0mV) 4'b0000: 0 mV 4'b0001: -20 mV 4'b0010: -40 mV 4'b0011: -60 mV 4'b0100: -80 mV 4'b0101: -100 mV 4'b0110: -120 mV 4'b0111: -140 mV 4'b1000: 160 mV 4'b1001: 140 mV 4'b1010: 120 mV 4'b1011: 100 mV 4'b1100: 80 mV 4'b1101: 60 mV 4'b1110: 40 mV 4'b1111: 20 mV

0ADA **SLDO_ANA_CON8** **SLDO control register 8** **0250**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VSRA	RG_VSRA	RG_VSRAM_PROC_ND								

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Name						M_PROC_PLCUR_EN	M_PROC_NDIS_EN	IS_PLCUR								
Type						RW	RW	RW								
Reset						0	1	0	0							

Bit(s)	Name	Description
10	RG_VSRAM_PROC_PLCUR_EN	**VSRAM fast-transient improve** 0: disable. 1: enable.
9	RG_VSRAM_PROC_NDIS_EN	**LDO output power down NMOS DISCHARGE Enable** 1'b0: disable output powerdown 1'b1: enable output powerdown
8:7	RG_VSRAM_PROC_NDIS_PLCUR	**Discharge current select for DVFS tracking** (2'b00: 100mA) 2'b00: 100mA 2'b01: 130mA 2'b10: 130mA 2'b11: 160mA

0ADC SLDO_ANA_CON9 SLDO control register 9 03FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_SLDO_RSV_H									
Type							RW									
Reset							1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
9:0	RG_SLDO_RSV_H	**Reserve level shift(default High)**

0ADE SLDO_ANA_CON10 SLDO control register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_SLDO_RSV_L									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	RG_SLDO_RSV_L	**Reserve level shift(default Low)**

0C00 OTP_CON0 OTP control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_OTP_PA					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
5:0	RG_OTP_PA	**OTP PA**

0C02 **OTP_CON1** **OTP control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_OTP_PDIN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RG_OTP_PDIN	**OTP PDIN**

0C04 **OTP_CON2** **OTP control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_OTP_PTM	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_OTP_PTM	**OTP PTM**

0C06 **OTP_CON3** **OTP control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_OTP_PWE	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_OTP_PWE	**OTP PWE**

0C08 **OTP_CON4** **OTP control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_PPROG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_PPROG	**OTP PPROG**

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0C0A **OTP_CON5** **OTP control register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_PWE_SRC
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_PWE_SRC	**OTP write(fusing) PWE source selection** 0: from IO pad 1: from register

0C0C **OTP_CON6** **OTP control register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_PROG_PKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_PROG_PKEY	**OTP write(fusing) match key**

0C0E **OTP_CON7** **OTP control register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_RD_PKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_RD_PKEY	**OTP read match key**

0C10 **OTP_CON8** **OTP control register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_RD_TRIG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_RD_TRIG	**OTP SW read trigger**

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0C12 OTP_CON9 OTP control register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_RD_RDY_BYPASS
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_RD_RDY_BYPASS	**Bypass OTP read ready delay** 0: not bypass 1: bypass

0C14 OTP_CON10 OTP control register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_SKIP_OTP_OUT
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_SKIP_OTP_OUT	**Skip reading from EFUSE macro** 0: not skip 1: skip

0C16 OTP_CON11 OTP control register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_RD_SW
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_RD_SW	**SW trigger read mode** 0: non SW trigger read mode 1: SW trigger read mode

0C18 OTP_CON12 OTP control register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_SW															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_SW	**Cuurent SW trigger read value**

0C1A **OTP_CON13** **OTP control register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_OTP_RD_ACK		RG_OTP_RD_BUSY
Type														RO		RO
Reset														0		0

Bit(s)	Name	Description
2	RG_OTP_RD_ACK	**OTP read ack**
0	RG_OTP_RD_BUSY	**OTP busy status**

0C1C **OTP_CON14** **OTP control register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_OTP_PA_SW				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RG_OTP_PA_SW	**Current SW trigger read row**

0C1E **OTP_DOUT_0_15** **OTP dout 0 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_0_15	

0C20 **OTP_DOUT_16_31** **OTP dout 16 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_16_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_16_31	

0C22 **OTP_DOUT_32_47** **OTP dout 32 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_32_47															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_32_47	

0C24 **OTP_DOUT_48_63** **OTP dout 48 63** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_48_63															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_48_63	

0C26 **OTP_DOUT_64_79** **OTP dout 64 79** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_64_79															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_64_79	

0C28 **OTP_DOUT_80_95** **OTP dout 80 95** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_80_95															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_80_95	

0C2A **OTP_DOUT_96_111** **OTP dout 96 111** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_96_111															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_96_111	

0C2C **OTP_DOUT_112_127** **OTP dout 112 127** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_112_127															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_112_127	

0C2E **OTP_DOUT_128_143** **OTP dout 128 143** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_128_143															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_128_143	

0C30 **OTP_DOUT_144_159** **OTP dout 144 159** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_144_159															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_144_159	

0C32 OTP_DOUT_160_175 OTP dout 160 175 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_160_175															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_160_175	

0C34 OTP_DOUT_176_191 OTP dout 176 191 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_176_191															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_176_191	

0C36 OTP_DOUT_192_207 OTP dout 192 207 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_192_207															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_192_207	

0C38 OTP_DOUT_208_223 OTP dout 208 223 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_208_223															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_208_223	

0C3A **OTP_DOUT_224_239** **OTP dout 224 239** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_224_239															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_224_239	

0C3C **OTP_DOUT_240_255** **OTP dout 240 255** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_240_255															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_240_255	

0C3E **OTP_DOUT_256_271** **OTP dout 256 271** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_256_271															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_256_271	

0C40 **OTP_DOUT_272_287** **OTP dout 272 287** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_272_287															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_272_287	

0C42 **OTP_DOUT_288_303** **OTP dout 288 303** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_288_303															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_288_303	

0C44 **OTP_DOUT_304_319** **OTP dout 304 319** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_304_319															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_304_319	

0C46 **OTP_DOUT_320_335** **OTP dout 320 335** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_320_335															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_320_335	

0C48 **OTP_DOUT_336_351** **OTP dout 336 351** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_336_351															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_336_351	

0C4A **OTP_DOUT_352_367** OTP dout 352 367 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_352_367															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_352_367	

0C4C **OTP_DOUT_368_383** OTP dout 368 383 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_368_383															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_368_383	

0C4E **OTP_DOUT_384_399** OTP dout 384 399 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_384_399															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_384_399	

0C50 **OTP_DOUT_400_415** OTP dout 400 415 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_400_415															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_400_415	

0C52 **OTP_DOUT_416_431** **OTP dout 416 431** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_416_431															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_416_431	

0C54 **OTP_DOUT_432_447** **OTP dout 432 447** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_432_447															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_432_447	

0C56 **OTP_DOUT_448_463** **OTP dout 448 463** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_448_463															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_448_463	

0C58 **OTP_DOUT_464_479** **OTP dout 464 479** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_464_479															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_464_479	

0C5A **OTP_DOUT_480_495** **OTP dout 480 495** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_480_495															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_480_495	

0C5C **OTP_DOUT_496_511** **OTP dout 496 511** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_496_511															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_496_511	

0C5E **OTP_VAL_0_15** **OTP val 0 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_0_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_0_15	

0C60 **OTP_VAL_16_31** **OTP val 16 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_16_31															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	RG_OTP_VAL_16_31	

0C62 OTP_VAL_32_47 OTP val 32 47 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_32_47															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_32_47	

0C64 OTP_VAL_48_63 OTP val 48 63 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_48_63															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_48_63	

0C66 OTP_VAL_64_79 OTP val 64 79 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_64_79															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_64_79	

0C68 OTP_VAL_80_95 OTP val 80 95 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_80_95															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_80_95	

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0C6A **OTP_VAL_96_111** **OTP val 96 111** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_96_111															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_96_111	

0C6C **OTP_VAL_112_127** **OTP val 112 127** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_112_127															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_112_127	

0C6E **OTP_VAL_128_143** **OTP val 128 143** **00D0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_128_143															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_128_143	

0C70 **OTP_VAL_144_159** **OTP val 144 159** **0D80**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_144_159															
Type	RW															
Reset	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_144_159	

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0C72 **OTP_VAL_160_175** **OTP val 160 175** **0008**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_160_175															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_160_175	

0C74 **OTP_VAL_176_191** **OTP val 176 191** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_176_191															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_176_191	

0C76 **OTP_VAL_192_207** **OTP val 192 207** **0008**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_192_207															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_192_207	

0C78 **OTP_VAL_208_223** **OTP val 208 223** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_208_223															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_208_223	

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0C7A **OTP_VAL_224_239** **OTP val 224 239** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_224_239															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_224_239	

0C7C **OTP_VAL_240_255** **OTP val 240 255** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_240_255															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_240_255	

0C7E **OTP_VAL_256_271** **OTP val 256 271** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_256_271															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_256_271	

0C80 **OTP_VAL_272_287** **OTP val 272 287** **0028**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_272_287															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_272_287	

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0C82 **OTP_VAL_288_303** **OTP val 288 303** **9100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_288_303															
Type	RW															
Reset	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_288_303	

0C84 **OTP_VAL_304_319** **OTP val 304 319** **4210**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_304_319															
Type	RW															
Reset	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_304_319	

0C86 **OTP_VAL_320_335** **OTP val 320 335** **0842**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_320_335															
Type	RW															
Reset	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_320_335	

0C88 **OTP_VAL_336_351** **OTP val 336 351** **0301**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_336_351															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	RG_OTP_VAL_336_351	

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0C8A **OTP_VAL_352_367** **OTP val 352 367** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_352_367															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_352_367	

0C8C **OTP_VAL_368_383** **OTP val 368 383** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_368_383															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_368_383	

0C8E **OTP_VAL_384_399** **OTP val 384 399** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_384_399															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_384_399	

0C90 **OTP_VAL_400_415** **OTP val 400 415** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_400_415															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_400_415	

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0C92 **OTP_VAL_416_431** **OTP val 416 431** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_416_431															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_416_431	

0C94 **OTP_VAL_432_447** **OTP val 432 447** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_432_447															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_432_447	

0C96 **OTP_VAL_448_463** **OTP val 448 463** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_448_463															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_448_463	

0C98 **OTP_VAL_464_479** **OTP val 464 479** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_464_479															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_464_479	

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0C9A **OTP_VAL_480_495** **OTP val 480 495** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_480_495															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_480_495	

0C9C **OTP_VAL_496_511** **OTP val 496 511** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_496_511															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_496_511	

0CA6 **FGADC_CON1** **FGADC control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_34_19															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_34_19	**Current charge value[34:19]**

0CA8 **FGADC_CON2** **FGADC control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_18_03															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_18_03	**Current charge value[18:3]**

0CAA **FGADC_CON3** **FGADC control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FG_CAR_02_00		
Type														RO		

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Reset														0	0	0

Bit(s)	Name	Description
2:0	FG_CAR_02_00	**Current charge value[2:0]**

0CAC FGADC_CON4 FGADC control register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_32_17															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_32_17	**Current charge time value[32:17]**

0CAE FGADC_CON5 FGADC control register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_16_01															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_16_01	**Current charge time value[16:1]**

0CB0 FGADC_CON6 FGADC control register 6 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FG_NTER_00
Type																RO
Reset																0

Bit(s)	Name	Description
0	FG_NTER_00	**Current charge time value[0]**

0CBA FGADC_CON11 FGADC control register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CURRENT_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CURRENT_OUT	**Current output charge of first stage[15:0]**

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0CC0 FGADC_CON14 FGADC control register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_FGANALOGTEST			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_FGANALOGTEST	**FGADC test bits**

0CF2 AUDDEC_ANA_CON0 AUDDEC control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPRSCDISABLE_VAUDP15	RG_AUDHPLSCDISABLE_VAUDP15	RG_AUDHSSCDISABLE_VAUDP15	RG_AUDHPRMUXINPUTSEL_VAUDP15		RG_AUDHPLMUXINPUTSEL_VAUDP15		RG_AUDHSMUXINPUTSEL_VAUDP15		RG_AUDHPRPWRUP_VAUDP15	RG_AUDHPLPWRUP_VAUDP15	RG_AUDHSPWRUP_VAUDP15	RG_AUD_DAC_PWL_UP_VA28	RG_AUD_DAC_PWR_UP_VA28	RG_AUDDACRPWRUP_VAUDP15	RG_AUDDACLPWRUP_VAUDP15
Type	RW	RW	RW	RW		RW		RW		RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_AUDHPRSCDISABLE_VAUDP15	**Headphone right short circuit protection disable**
14	RG_AUDHPLSCDISABLE_VAUDP15	**Headphone left short circuit protection disable**
13	RG_AUDHSSCDISABLE_VAUDP15	**Headset short circuit protection disable**
12:11	RG_AUDHPRMUXINPUTSEL_VAUDP15	**Audio right headphone input multiplexor selection, positive/negative pins:** (00) open / open, (01) LoudSPK playback, (10) Audio playback, (11): test mode
10:9	RG_AUDHPLMUXINPUTSEL_VAUDP15	**Audio left headphone input multiplexor selection, positive/negative pins:** (00) open / open, (01) LoudSPK playback, (10) Audio playback, (11): test mode
8:7	RG_AUDHSMUXINPUTSEL_VAUDP15	**Audio handset input multiplexor selection, positive/negative pins:** (00) open / open, (01) MUTE (Input grounded), (10) Voice playback, (11): test mode
6	RG_AUDHPRPWRUP_VAUDP15	**Audio right headphone power up**
5	RG_AUDHPLPWRUP_VAUDP15	**Audio left headphone power up**
4	RG_AUDHSPWRUP_VAUDP15	**Audio headset power up**
3	RG_AUD_DAC_PWL_UP_VA28	**Power down control for left channel audio biasgen. (0): power down, (1): enable**
2	RG_AUD_DAC_PWR_UP_VA28	**Power down control for right channel audio biasgen. (0): power down, (1): enable**
1	RG_AUDDACRPWRUP_VAUDP15	**Power down control for right-channel audio DAC. (0): power down, (1): enable**

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Bit(s)	Name	Description
0	RG_AUDDACLPWRUP_VAUDP15	**Power down control for left-channel audio DAC. (0): power down, (1): enable**

0CF4 **AUDDEC_ANA_CON1** **AUDDEC control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**RG_HSOUTPUTRESETo_VAUDP15**	**RG_HSINPUTRESETo_VAUDP15**	**RG_HSOUTPUTSTBENH_VAUDP15**	**RG_HSINPUTSTBENH_VAUDP15**	**RG_HPOUT_SHORTVCM_VAUDP15**	**RG_HPOUTPUTRESETo_VAUDP15**	**RG_HPINPUTRESETo_VAUDP15**	**RG_HPOUTPUTSTBENH_VAUDP15**	**RG_HPINPUTSTBENH_VAUDP15**	**RG_PRECHARGEBUF_EN_VAUDP15**	**RG_AUDHSSTARTUP_VAUDP15**	**RG_AUDHPSTARTUP_VAUDP15**	**RG_AUDHSBSCCURRENT_VAUDP15**	**RG_AUDHPRBSCCURRENT_VAUDP15**	**RG_AUDHPLBSCCURRENT_VAUDP15**
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_HSOUTPUTRESETo_VAUDP15	**HS driver DE outputs reset to 0V ground, (0): no reset, (1): reset**
13	RG_HSINPUTRESETo_VAUDP15	**HS driver DE inputs reset to 0V ground, (0): no reset, (1): reset**
12	RG_HSOUTPUTSTBENH_VAUDP15	**HS driver output stability enhance option, (0): no enhance, (1): enhance**
11	RG_HSINPUTSTBENH_VAUDP15	**HS driver input stability enhance option, (0): no enhance, (1): enhance**
10	RG_HPOUT_SHORTVCM_VAUDP15	**Short HP output to VCM (DCC: 0V; ACC: 1.4V), (0): not short to VCM, (1) short to VCM**
9	RG_HPOUTPUTRESETo_VAUDP15	**HPL/R driver SE output reset to 0V ground, (0): no reset, (1): reset**
8	RG_HPINPUTRESETo_VAUDP15	**HP driver input reset to ground, (0): no reset, (1): reset**
7	RG_HPOUTPUTSTBENH_VAUDP15	**HP driver output stability enhance option, (0): no enhance, (1): enhance**
6	RG_HPINPUTSTBENH_VAUDP15	**HP driver input stability enhance option, (0): no enhance, (1): enhance**
5	RG_PRECHARGEBUF_EN_VAUDP15	**Pre-charge buffer stage2 enable, (0): disable, (1): enable**
4	RG_AUDHSSTARTUP_VAUDP15	**Forces a Startup mode in HS Amp if required**
3	RG_AUDHPSTARTUP_VAUDP15	**Forces a Startup mode in HP Amps if required**
2	RG_AUDHSBSCCURRENT_VAUDP15	**Audio handset BSC current**
1	RG_AUDHPRBSCCURRENT_VAUDP15	**Audio right headphone BSC current**
0	RG_AUDHPLBSCCURRENT_VAUDP15	**Audio left headphone BSC current**

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0CF6 **AUDDEC_ANA_CON2** **AUDDEC control register 2** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPRFINETRIM_VAUDP15		RG_AUDHPLFINETRIM_VAUDP15		RG_AUDHPTRIM_EN_VAUDP15	RG_AUDHPRTRIM_VAUDP15				RG_AUDHPLTRIM_VAUDP15				RG_HSOUT_SHORTVCM_VAUDP15	RG_HPOUTSTB_RSEL_VAUDP15	
Type	RW		RW		RW	RW				RW				RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:14	RG_AUDHPRFINETRIM_VAUDP15	Fine trim offset voltage of HPR. (01): -0.5mV, (10): +0.5mV
13:12	RG_AUDHPLFINETRIM_VAUDP15	Fine trim offset voltage of HPL. (01): -0.5mV, (10): +0.5mV
11	RG_AUDHPTRIM_EN_VAUDP15	Enable control of trim circuit of HP. (0): disable trim circuit (1): enable trim circuit
10:7	RG_AUDHPRTRIM_VAUDP15	Trim offset voltage of HPR. (0000): 0V, (0001): -0.5mV, (0010): -1.5mV, (0011): -2.5mV, (0100): -3.5mV, (0101): -4.5mV, (0110): -5.5mV, (0111): -6.5mV; (1001): 0.5mV, (1010): 1.5mV, (1011): 2.5mV, (1100): 3.5mV, (1101): 4.5mV, (1110): 5.5mV, (1111): 6.5mV
6:3	RG_AUDHPLTRIM_VAUDP15	Trim offset voltage of HPL. (0000): 0V, (0001): -0.5mV, (0010): -1.5mV, (0011): -2.5mV, (0100): -3.5mV, (0101): -4.5mV, (0110): -5.5mV, (0111): -6.5mV; (1001): 0.5mV, (1010): 1.5mV, (1011): 2.5mV, (1100): 3.5mV, (1101): 4.5mV, (1110): 5.5mV, (1111): 6.5mV
2	RG_HSOUT_SHORTVCM_VAUDP15	Short HS output to VCM (DCC: 0V; ACC: 1.4V), (0): not short to VCM, (1) short to VCM
1:0	RG_HPOUTSTB_RSEL_VAUDP15	Selection of OUTSTB resistance. (00):250, (01):470, (10):1.5k

0CF8 **AUDDEC_ANA_CON3** **AUDDEC control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP15		RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP15		RG_AUDHPSPKDET_EN_VAUDP15	RG_AUDTRIMBUF_GAINSEL_VAUDP15		RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP15				RG_AUDTRIMBUF_EN_VAUDP15
Type					RW		RW		RW	RW		RW				RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:10	RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP15	Audio headphone speaker detection output mux selection: (00)Open, (01)HPL, (10)HPR, (11) Unused
9:8	RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP15	Audio headphone speaker detection input mux enable: (00)Open, (01)DACLP, (10)DACLN, (11)DACRP
7	RG_AUDHPSPKDET_	Audio headphone speaker detection enable

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Bit(s)	Name	Description
	EN_VAUDP15	
6:5	RG_AUDTRIMBUF_GAINSEL_VAUDP15	**Audio offset trimming buffer gain selection: (00)0dB, (01)6dB, (10)12dB, (11)18dB**
4:1	RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP15	**Audio offset trimming buffer mux selection: (0000)open, (0001)HPL, (0010)HPR, (0011)HSP, (0100)HSN,** (0101)IV_P, (0110)IV_N, (0111)AVSS32, (1000)AVSS32, (1001)AVSS32, (1010~1111)Unused
0	RG_AUDTRIMBUF_EN_VAUDP15	**Audio offset trimming buffer enable**

0CFA **AUDDEC_ANA_CON4** **AUDDEC control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RESERVED_VAUDP15								RG_ABIDEC_RESERVED_VA28							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RESERVED_VAUDP15	**Reserved one byte in VAUDP15 domain**
7:0	RG_ABIDEC_RESERVED_VA28	**Reserved one byte in VA28 domain**

0CFC **AUDDEC_ANA_CON5** **AUDDEC control register 5** **5520**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDBIASADJ_1_VAUDP15						RG_AUDBIASADJ_0_VAUDP15									
Type	RW						RW									
Reset	0	1	0	1	0	1	0	1	0	0	1	0				

Bit(s)	Name	Description
15:10	RG_AUDBIASADJ_1_VAUDP15	**Audio bias adjustment 1, bits: [5:4] ZCD bias current setting (00) 3uA, (01) 4uA, (10) 5uA, (11) 6uA** [3:2] HS ibias setting, (00) 4uA, (01) 5uA, (10) 6uA, (11) 7uA [1:0]: HPL/R ibias setting, (00) 4uA, (01) 5uA, (10) 6uA, (11) 7uA
9:4	RG_AUDBIASADJ_0_VAUDP15	**Audio bias adjustment 0, bits: [2:0] Headphone Left/Right DR bias current setting, [5:3] Handset DR bias current setting. DR bias settings: (000) 4uA, (001) 5uA, (010) 6uA, (011) 7uA, (100) 8uA, (101) 9A, (110) 10uA, (111) 11uA,**

0CFE **AUDDEC_ANA_CON6** **AUDDEC control register 6** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_HCLDO_VOSE	RG_LCLDO_VOSEL_V	RG_LCLDO_REMOT	RG_LCLDO_PDDIS_E	RG_HCLDO_REMOT	RG_HCLDO_PDDIS_	RG_VA33REFGEN_EN	RG_LCLDO_ENC_EN_	RG_LCLDO_EN_VA18	RG_HCLDO_EN_VA1	RG_SEL_DELAY_VCO	RG_SEL_ENCODER_	RG_SEL_DECODER_9	RG_RSTB_ENCODER_	RG_RSTB_DECODER_	RG_AUDIBIASPWRD

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	L_VA18	A18	E_SENSE_VA18	N_VA18	E_SENSE_VA18	EN_VA18	_VA18	VA28		8	RE	96K_VA28	6K_VA28	VA28	VA28	N_VAUDP15
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	RG_HCLDO_VOSEL_VA18	
14	RG_LCLDO_VOSEL_VA18	
13	RG_LCLDO_REMOTE_SENSE_VA18	**LCLDO Remote sense function selection, 0: local sense, 1: remote sense**
12	RG_LCLDO_PDDIS_EN_VA18	**LCLDO Power Down Discharge Enable**
11	RG_HCLDO_REMOTE_SENSE_VA18	**HCLDO Remote sense function selection, 0: local sense, 1: remote sense**
10	RG_HCLDO_PDDIS_EN_VA18	**HCLDO Power Down Discharge Enable**
9	RG_VA33REFGEN_EN_VA18	
8	RG_LCLDO_ENC_EN_VA28	**Enable for LCLDO_ENC**
7	RG_LCLDO_EN_VA18	**Enable for LCLDO**
6	RG_HCLDO_EN_VA18	**Enable for HCLDO**
5	RG_SEL_DELAY_VCORE	**AFIFO read clock delay selection, (0):5ns, (1):10ns**
4	RG_SEL_ENCODER_96K_VA28	**Audio ADC clock selection, (0): 6.5MHz; (1): 13MHz**
3	RG_SEL_DECODER_96K_VA28	**Audio DAC clock selection, (0): 6.5MHz; (1): 13MHz**
2	RG_RSTB_ENCODER_VA28	**Audio encoder reset, (0): reset; (1): normal**
1	RG_RSTB_DECODER_VA28	**Audio decoder reset, (0): reset; (1): normal**
0	RG_AUDIBIASPWRDN_VAUDP15	**Power down control for IbiasDistrib circuit. (0): enable, (1): disable**

0D00 **AUDDEC_ANA_CON7** **AUDDEC control register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_NVREG_EN_VAUDP15	RG_AUDPMU_RESERVED_VAUDP15				RG_AUDPMU_RESERVED_VA18				RG_AUDPMU_RESERVED_VA28				RG_VA28REFGEN_EN_VA28	RG_LCLDO_ENC_REMOTE_SENSE_VA28	RG_LCLDO_ENC_PDDIS_EN_VA28
Type	RW	RW				RW				RW				RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	RG_NVREG_EN_VAUDP15	**Enable for NVREG**
14:11	RG_AUDPMU_RESERVED_VAUDP15	**Reserved half byte for VAUDP15 domain**
10:7	RG_AUDPMU_RESERVED_VA18	**Reserved half byte for VA18 domain**
6:3	RG_AUDPMU_RESERVED_VA28	**Reserved half byte for VA28 domain**
2	RG_VA28REFGEN_EN_VA28	**Enable VA28 Ref. gen.**
1	RG_LCLDO_ENC_REMOTE_SENSE_VA28	**LCLDO_ENC Remote Sense Function Selection, (0): Local Sense, (1): Remote Sense**
0	RG_LCLDO_ENC_PDDIS_EN_VA28	**LCLDO_ENC Power Down Discharge Enable**

0D02 AUDDEC_ANA_CON8 AUDDEC control register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_AUDGLB_PWRDN_VA28	RG_NVREG_PULL0V_VAUDP15
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_AUDGLB_PWRDN_VA28	**Power down control for audio global bias circuit, (0): enable, (1): disable; default on**
0	RG_NVREG_PULL0V_VAUDP15	**(0): DCC mode, switch is opened, NV output is -0.95V; (1): ACC mode, switch is closed, NV reg output is pulled to GND**

0D04 AUDENC_ANA_CON0 AUDENC control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDADCLINPUTSEL		RG_AUDADCLPWRUP	RG_AUDPREAMPLINPUTSEL		RG_AUDPREAMPLVSCALE		RG_AUDPREAMPLPGATEST	RG_AUDPREAMPLDCPRECHARGE	RG_AUDPREAMPLDCEN	RG_AUDPREAMPLON
Type						RW		RW	RW		RW		RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:9	RG_AUDADCLINPUTSEL	**Audio L ADC input selection:** (00) Idle, (01) AIN0, (10) Left Preamplifier, (11) Idle
8	RG_AUDADCLPWRU	**Audio L ADC power up**

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Bit(s)	Name	Description
	P	0 Power down. 1 Power on.
7:6	RG_AUDPREAMPLINPUTSEL	**Audio L preamplifier input selection:** (00) None, (01) AIN0, (10) AIN1, (11) AIN2.
5:4	RG_AUDPREAMPLVSCALE	**Audio L preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPLPGATEST	**Audio L preamplifier PGA test enable** 0 disable 1 enable
2	RG_AUDPREAMPLDCRPECHARGE	**Audio L preamplifier PGA DC couple input precharge** 0 disable 1 enable
1	RG_AUDPREAMPLDCCEN	**Audio L DC couple input** 0 AC couple input 1 DC couple input
0	RG_AUDPREAMPLON	**Audio L preamplifier enable** 0 disable 1 enable

0D06 **AUDENC_ANA_CON1** **AUDENC control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDADCRINPUTSEL		RG_AUDADCRPWRUP	RG_AUDPREAMPRINPUTSEL		RG_AUDPREAMPRVSCALE		RG_AUDPREAMPRPGATEST	RG_AUDPREAMPRDCRPECHARGE	RG_AUDPREAMPRDCCEN	RG_AUDPREAMPRON
Type						RW		RW	RW		RW		RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:9	RG_AUDADCRINPUTSEL	**Audio R ADC input selection:** (00) Idle, (01) AIN0, (10) Right Preamplifier, (11) Idle
8	RG_AUDADCRPWRUP	**Audio R ADC power up** 0 Power down. 1 Power on.
7:6	RG_AUDPREAMPRINPUTSEL	**Audio R preamplifier input selection:** (00) None, (01) AIN0, (10) AIN1, (11) AIN2.
5:4	RG_AUDPREAMPRVSCALE	**Audio R preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPRPGATEST	**Audio R preamplifier PGA test enable** 0 disable 1 enable
2	RG_AUDPREAMPRDCRPECHARGE	**Audio R preamplifier PGA DC couple input precharge** 0 disable 1 enable
1	RG_AUDPREAMPRDCCEN	**Audio R DC couple input** 0 AC couple input 1 DC couple input

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Bit(s)	Name	Description
0	RG_AUDPREAMPRON	**Audio R preamplifier enable** 0 disable 1 enable

0D08 **AUDENC_ANA_CON2** **AUDENC control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCFLASHIDDTEST		RG_AUDADCREFBUFIDDTEST		RG_AUDADC2NDSTAGEIDDTEST		RG_AUDADC1STSTAGEIDDTEST		RG_AUDPREAMPIDDTEST		RG_AUDADCFLASHLPEN	RG_AUDADC2NDSTAGELPEN	RG_AUDADC1STSTAGELPEN	RG_AUDPREAMPLPEN	RG_AUDGLBMADLPWEN	RG_AUDULHALFBIAS
Type	RW		RW		RW		RW		RW		RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_AUDADCFLASHIDDTEST	**Audio ADC flash Idd current test selection** 00: 100% 01: 80% 10: 120% 11: 140%
13:12	RG_AUDADCREFBUFIDDTEST	**Audio ADC reference buffer Idd current test selection** 00: 100% 01: 80% 10: 120% 11: 140%
11:10	RG_AUDADC2NDSTAGEIDDTEST	**Audio ADC 2nd & 3rd Stage Idd adjust bits** 00: 100% 01: 80% 10: 120% 11: 140%
9:8	RG_AUDADC1STSTAGEIDDTEST	**Audio ADC 1st Stage Idd adjust bits** 00: 100% 01: 80% 10: 120% 11: 140%
7:6	RG_AUDPREAMPIDDTEST	**Audio preamplifier Idd adjust bits** 00: 100% 01: 75% 10: 125% 11: 150%
5	RG_AUDADCFLASHLPEN	**Audio ADC flash low power enable** 0 normal 1 enable
4	RG_AUDADC2NDSTAGELPEN	**Audio ADC 2nd & 3rd low power enable** 0 normal 1 enable
3	RG_AUDADC1STSTAGELPEN	**Audio ADC 1st Stage low power enable** 0 normal 1 enable
2	RG_AUDPREAMPLPEN	**Audio preamplifier PGA low power mode** 0 disable

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Bit(s)	Name	Description
		1 enable
1	RG_AUDGLBMADLPWEN	**Audio uplink globe bias VOW low power mode enable** 0 normal 1 enable
0	RG_AUDULHALFBIAS	**Audio uplink halfbias enable** 0 normal 1 enable

0D0A **AUDENC_ANA_CON3** **AUDENC control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDSPAREPGA	RG_DCCVCMBUFLPSWEN	RG_DCCVCMBUFLPMODSEL	RG_AUDPREAMPAAFEN			RG_AUDADCCLKGENMODE		RG_AUDADCCLKSOURCE		RG_AUDADCCLKSEL	RG_AUDADCDAC0P25FS
Type					RW	RW	RW	RW			RW		RW		RW	RW
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_AUDSPAREPGA	**Spare control bits for PGA**
10	RG_DCCVCMBUFLPSWEN	**Audio preamplifier PGA DCC VCM buffer SW EN**
9	RG_DCCVCMBUFLPMODSEL	**Audio preamplifier PGA DCC VCM buffer LP MODSEL**
8	RG_AUDPREAMPAAFEN	**Audio preamplifier PGA with AAF input in DC couple mode** 0 disable 1 enable
5:4	RG_AUDADCCLKGENMODE	**Audio ADC clock gen. mode** 00: divided by 2 (Normal) 01: divided by 4 10: divided by 8 11: No divided
3:2	RG_AUDADCCLKSOURCE	**Audio ADC clock source** 00 26MHz from CLKSQ 01 12.58MHz from 32KHz PLL 10 12MHz Ring oscillator 11 None
1	RG_AUDADCCLKSEL	**Audio ADC clock selection** 0 13MHz clock in, 6.5MHz data out 1 26MHz clock in, 13MHz data out
0	RG_AUDADCDAC0P25FS	**Audio ADC FBDAC 0.25FS enable** 0 13MHz clock in, 6.5MHz data out 1 3.25MHz clock in, 1.625MHz data out

0D0C **AUDENC_ANA_CON4** **AUDENC control register 4** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_A	RG_A	RG_A	RG_AUDAD		RG_A	RG_A	RG_A	RG_A	RG_A	RG_A	RG_A	RG_A	RG_A

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			UDADCDACTEST	UDADCNODEM	UDADCDACNRZ	CDACIDDTEST		UDADCDACFBCURRENT	UDADCFFBYPASS	UDADCBYPASS	UDADCNOPATEST	UDADCWIDECM	UDADCFSRESET	UDADC3RDSTAGERESET	UDADC2NDSTAGERESET	UDADC1STSTAGESDENB
Type			RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	RG_AUDADCDACTEST	**Audio ADC DAC test** 0 disable 1 enables the data in RG_AUDADCTESTDATA[15:0] to be passed to the DAC
12	RG_AUDADCNODEM	**Audio ADC DEM test**
11	RG_AUDADCDACNRZ	**Audio ADC DAC in non return to zero mode** 0 RZ mode (2I) 1 NRZ mod (I)
10:9	RG_AUDADCDACIDDTEST	**Audio ADC-DAC Idd current test selfection** 00 Normal 11 -20% DAC f/b current
8	RG_AUDADCDACFBCURRENT	**Audio ADC feedback coefficient**
7	RG_AUDADCFFBYPASS	**Audio ADC feed forward bypass** 0 no bypass, allow feedforward coefficient to pass signal to ADC flash 1 bypass, don't allow ADC i/p signal to feedforward flash
6	RG_AUDADCBYPASS	**Audio ADC input resistor bypass enable** 0 disable 1 enable
5	RG_AUDADCNOPATEST	**Audio ADC no preamp test** 0 Normal ADC Gain 1 6dB ADC Gain
4	RG_AUDADCWIDECM	**Audio ADC wide common mode enable** 0 normal 1 enable
3	RG_AUDADCFSRESET	**Audio encoder FS reset block model selection**
2	RG_AUDADC3RDSTAGERESET	**Audio ADC 3rd stage reset** 0 normal 1 Reset
1	RG_AUDADC2NDSTAGERESET	**Audio ADC 2nd stage reset** 0 normal 1 Reset
0	RG_AUDADC1STSTAGESDENB	**Audio ADC 1st stage source degenerate enableb** 0 Enable 1 Disable

0D0E **AUDENC_ANA_CON5** **AUDENC control register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCTESTDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_AUDADCTESTDATA	**Audio ADC test data bits** Audio ADC test data bits for both phases of DRTZ DAC. Can enable any current source you choose.

0D10 **AUDENC_ANA_CON6** **AUDENC control register 6** **0555**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDRCTUNERSEL			RG_AUDRCTUNER					RG_AUDRCTUNELSEL	RG_AUDRCTUNEL				
Type			RW			RW					RW	RW				
Reset			0			1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
13	RG_AUDRCTUNERSEL	**Audio R ADC RC tuning select** 0 Use auto cal tune bits 1 use RG_AUDRCTUNEL[4:0]
10:6	RG_AUDRCTUNER	**Audio R ADC RC tuned value** See RG_AUDRCTUNELSE
5	RG_AUDRCTUNELSEL	**Audio L ADC RC tuning select** 0 Use auto cal tune bits 1 use RG_AUDRCTUNEL[4:0]
4:0	RG_AUDRCTUNEL	**Audio L ADC RC tuned value** See RG_AUDRCTUNELSE

0D12 **AUDENC_ANA_CON7** **AUDENC control register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDENCSPAREVA18				RG_AUDENCSPAREVA28				RG_AUDSPAREVA18				RG_AUDSPAREVA28			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	RG_AUDENCSPAREVA18	**Spare control bits for AVDD12 voltage domain**
11:8	RG_AUDENCSPAREVA28	**Spare control bits for AVDD25 voltage domain**
7:4	RG_AUDSPAREVA18	**Spare control bits for AVDD12 voltage domain**
3:0	RG_AUDSPAREVA28	**Spare control bits for AVDD25 voltage domain**

0D14 **AUDENC_ANA_CON8** **AUDENC control register 8** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RG_AUDSPAREVMIC				RG_DMICMONSEL			RG_DMICMONEN	RG_AUDDIGMICNDUTY		RG_AUDDIGMICPDUTY		RG_DMICHPCLKEN	RG_AUDDIGMICBIAS		RG_AUDDIGMICEN
Type	RW				RW			RW	RW		RW		RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:12	RG_AUDSPAREVMIC	**Spare control bits for AVDD25MIC voltage domain**
11:9	RG_DMICMONSEL	**Digital microphone monitor path**
8	RG_DMICMONEN	**Enable digital microphone monitor path** 0 disable 1 enable
7:6	RG_AUDDIGMICNDUTY	**Digital microphone negative duty control**
5:4	RG_AUDDIGMICPDUTY	**Digital microphone positive duty control**
3	RG_DMICHPCLKEN	**Digital microphone CLK source from** 0 Digital 1 CLKSQ
2:1	RG_AUDDIGMICBIAS	**Digital microphone slew rate control** 11>10>01>00
0	RG_AUDDIGMICEN	**Digital microphone enable** 0 disable 1 enable

0D16 AUDENC_ANA_CON9 AUDENC control register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_BANDGAPGEN	RG_AUDMICBIASLOWPEN	RG_AUDMICBIASVREF			RG_AUDMICBIAS1BYPASSEN	RG_AUDMICBIAS1DCSWNEN	RG_AUDMICBIAS1DCSWPEN	RG_AUDPWDBMICBIAS1	RG_AUDMICBIAS0BYPASSEN	RG_AUDMICBIAS0DCSWNEN	RG_AUDMICBIAS0DCSWPEN	RG_AUDPWDBMICBIAS0
Type				RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	RG_BANDGAPGEN	**remote sense to bandgap ground** 0: disable 1: enable
11	RG_AUDMICBIASLOWPEN	**MIC Bias 0 LowPower enable** 0: normal mode 1: low power mode
10:8	RG_AUDMICBIASVREF	**MIC Bias 0 Output voltage selection** 000: 1.7V, 001: 1.8V, 010: 1.9V, 011: 2.0V 100: 2.1V, 101: 2.3V, 110: 2.4V, 111: 2.5V
7	RG_AUDMICBIAS1BYPASSEN	**MIC Bias 1 BYPASS 2P8V EN** 0: disable 1: enable
6	RG_AUDMICBIAS1DCSWNEN	**MIC Bias 1 DC couple switch N** 0: external

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Bit(s)	Name	Description
		1: internal
5	RG_AUDMICBIAS1DCSWPEN	**MIC Bias 1 DC couple switch P** 0: external 1: internal
4	RG_AUDPWDBMICBIAS1	**MIC Bias 1 power down** 0: power down 1: power on
3	RG_AUDMICBIAS0BYPASSEN	**MIC Bias 0 BYPASS 2P8V EN** 0: disable 1: enable
2	RG_AUDMICBIAS0DCSWNEN	**MIC Bias 0 DC couple switch N** 0: external 1: internal
1	RG_AUDMICBIAS0DCSWPEN	**MIC Bias 0 DC couple switch P** 0: external 1: internal
0	RG_AUDPWDBMICBIAS0	**MIC Bias 0 power down** 0: power down 1: power on

0D18 **AUDENC_ANA_CON10** **AUDENC control register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_AUDPREAMPRGAIN				RG_AUDPREAMPLGAIN		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit(s)	Name	Description
6:4	RG_AUDPREAMPRGAIN	**Audio R preamplifier gain adjust:** (000) 0dB, (001) 6dB, (010) 12dB (011) 18dB, (100) 24dB
2:0	RG_AUDPREAMPLGAIN	**Audio L preamplifier gain adjust:** (000) 0dB, (001) 6dB, (010) 12dB (011) 18dB, (100) 24dB

0D1A **AUDNCP_CLKDIV_CON0** **AUDNCP_CLKDIV control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_CHG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_CHG	

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0D1C **AUDNCP_CLKDIV_CON1** **AUDNCP_CLKDIV control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_ON
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_ON	

0D1E **AUDNCP_CLKDIV_CON2** **AUDNCP_CLKDIV control register 2** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_DIVCKS_PRG								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
8:0	RG_DIVCKS_PRG	

0D20 **AUDNCP_CLKDIV_CON3** **AUDNCP_CLKDIV control register 3** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_PWD_NCP
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_DIVCKS_PWD_NCP	

0D22 **AUDNCP_CLKDIV_CON4** **AUDNCP_CLKDIV control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_DIVCKS_PWD_NCP_ST_SEL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1:0	RG_DIVCKS_PWD_NCP_ST_SEL	

0D24 DCXO_CW00 DCXO Code Word 0 6B6D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CLKSEL_MAN	XO_ENBB_EN_M	XO_ENBB_MAN	XO_BB_LPM_EN	XO_EXTBUF4_EN_M	XO_EXTBUF4_MODE		XO_EXTBUF3_EN_M	XO_EXTBUF3_MODE		XO_EXTBUF2_EN_M	XO_EXTBUF2_MODE		XO_EXTBUF1_EN_M	XO_EXTBUF1_MODE	
Type	RW	RW	RW	RW	RW	RW		RW	RW		RW	RW		RW	RW	
Reset	0	1	1	0	1	0	1	1	0	1	1	0	1	1	0	1

Bit(s)	Name	Description
15	XO_CLKSEL_MAN	**CLK_SEL Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
14	XO_ENBB_EN_M	**EN_BB Manual Control when XO_ENBB_MAN is 1** 0: EN_BB = 0 1: EN_BB = 1
13	XO_ENBB_MAN	**EN_BB Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
12	XO_BB_LPM_EN	**SW-Controlled Low-Power Mode for Saving Power during Transceiver Standby** 0: Disabled 1: Enabled
11	XO_EXTBUF4_EN_M	**XO_CEL 26MHz Clock Buffer Manual (Register) Control** 0: Disabled 1: Enabled
10:9	XO_EXTBUF4_MODE	**XO_CEL 26MHz Clock Buffer Control Signal Selection** 00: XO_EXTBUF1_EN_M 01: EN_BB 10: CLK_SEL 11: BUF24_EN
8	XO_EXTBUF3_EN_M	**XO_NFC 26MHz Clock Buffer Manual (Register) Control** 0: Disabled 1: Enabled
7:6	XO_EXTBUF3_MODE	**XO_NFC 26MHz Clock Buffer Control Signal Selection** 00: XO_EXTBUF1_EN_M 01: EN_BB 10: CLK_SEL 11: BUF234_EN
5	XO_EXTBUF2_EN_M	**XO_WCN 26MHz Clock Buffer Manual (Register) Control** 0: Disabled 1: Enabled
4:3	XO_EXTBUF2_MODE	**XO_WCN 26MHz Clock Buffer Control Signal Selection** 00: XO_EXTBUF1_EN_M 01: EN_BB 10: CLK_SEL 11: BUF24_EN
2	XO_EXTBUF1_EN_M	**XO_SOC 26MHz Clock Buffer Manual (Register) Control** 0: Disabled

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Bit(s)	Name	Description
		1: Enabled
1:0	XO_EXTBUF1_MODE	**XO_SOC 26MHz Clock Buffer Control Signal Selection** 00: XO_EXTBUF1_EN_M 01: EN_BB 10: CLK_SEL 11: EN_BB or CLK_SEL

0D26 **DCXO_CW00_SET** **DCXO Code Word 0 Set** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW00_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW00_SET	**DCXO Code Word 0 Set** 0: No Set 1: Set

0D28 **DCXO_CW00_CLR** **DCXO Code Word 0 Clear** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DCXO_CW00_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	DCXO_CW00_CLR	**DCXO Code Word 0 Clear** 0: No Clear 1: Clear

0D2A **DCXO_CW01** **DCXO Code Word 1** **ED55**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_AUDIO_EN_M	XO_LPBUF_EN_M	XO_LPM_PREBUF_EN_M	XO_LPMBUF_MAN	XO_IBUF_EN_M	XO_PBUF_EN_M	XO_INTBUF_MAN	XO_EXTBUF4_CKG_EN_M	XO_EXTBUF4_CKG_MAN	XO_EXTBUF3_CKG_EN_M	XO_EXTBUF3_CKG_MAN	XO_EXTBUF2_CKG_EN_M	XO_EXTBUF2_CKG_MAN	XO_EXTBUF1_CKG_EN_M	XO_EXTBUF1_CKG_MAN	XO_CLKSEL_EN_M
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	0	1	1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
15	XO_AUDIO_EN_M	**Audio 26MHz Clock Output Manual Control when XO_LPMBUF_MAN is 1** 0: Disabled 1: Enabled
14	XO_LPBUF_EN_M	**XO Low-Power Buffer Manual Control when XO_LPMBUF_MAN is**

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Bit(s)	Name	Description
		1 0: Disabled 1: Enabled
13	XO_LPM_PREBUF_EN_M	**XO Low-Power Buffer Bias Manual Control when XO_LPMBUF_MAN is 1** 0: Disabled 1: Enabled
12	XO_LPMBUF_MAN	**XO Low-Power Buffer Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
11	XO_IBUF_EN_M	**XO Isolated Buffer Manual Control when XO_INTBUF_MAN is 1** 0: Disabled 1: Enabled
10	XO_PBUF_EN_M	**XO Pre-buffer Manual Control when XO_INTBUF_MAN is 1** 0: Disabled 1: Enabled
9	XO_INTBUF_MAN	**XO Internal Buffer Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
8	XO_EXTBUF4_CKG_EN_M	**XO_CEL 26MHz Clock Output Manual Control when XO_EXTBUF4_CKG_MAN is 1** 0: Disabled 1: Enabled
7	XO_EXTBUF4_CKG_MAN	**XO_CEL 26MHz Clock Output Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
6	XO_EXTBUF3_CKG_EN_M	**XO_NFC 26MHz Clock Output Manual Control when XO_EXTBUF3_CKG_MAN is 1** 0: Disabled 1: Enabled
5	XO_EXTBUF3_CKG_MAN	**XO_NFC 26MHz Clock Output Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
4	XO_EXTBUF2_CKG_EN_M	**XO_WCN 26MHz Clock Output Manual Control when XO_EXTBUF2_CKG_MAN is 1** 0: Disabled 1: Enabled
3	XO_EXTBUF2_CKG_MAN	**XO_WCN 26MHz Clock Output Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
2	XO_EXTBUF1_CKG_EN_M	**XO_SOC 26MHz Clock Output Manual Control when XO_EXTBUF1_CKG_MAN is 1** 0: Disabled 1: Enabled
1	XO_EXTBUF1_CKG_MAN	**XO_SOC 26MHz Clock Output Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
0	XO_CLKSEL_EN_M	**CLK_SEL Manual Control when XO_CLKSEL_MAN is 1** 0: CLK_SEL = 0 1: CLK_SEL = 1

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0D2C **DCXO_CW02** **DCXO Code Word 2** **386A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_OPMODE_MAN	XO_26MLP_MAN_EN	XO_CBANK_SYNC_DYN	XO_LDOCAL_EN	XO_EN26M_OFFSQ_EN	XO_AAC_MODE_FPM		XO_AAC_MODE_LPM		XO_AAC_FPM_TIME		XO_STRUP_MODE	XO_XMODE_M	XO_XMODE_MAN	XO_EN32K_M	XO_EN32K_MAN
Type	RW	RW	RW	RW	RW	RW		RW		RW		RW	RW	RW	RW	RW
Reset	0	0	1	1	1	0	0	0	0	1	1	0	1	0	1	0

Bit(s)	Name	Description
15	XO_OPMODE_MAN	**XO Pre-buffer Dithering Delay Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
14	XO_26MLP_MAN_EN	**DA_XO_26MLP_EN Control Mode** 0: HW-Control Mode 1: DA_XO_26MLP_EN = 1
13	XO_CBANK_SYNC_DYN	**Control of Updating Clock of CBANK** 0: Updating Clock of CBANK Keeps on 1: Updating Clock of CBANK Turns on when CDAC Gets Updated
12	XO_LDOCAL_EN	**FPM LDO Calibration Mode** 0: Keeping Previous FPM LDO Voltage Setting 1: Triggering FPM LDO Calibration when Entering FPM
11	XO_EN26M_OFFSQ_EN	**Off Sequence Control when 26M_EN is 0** 0: Disabled 1: Enabled
10:9	XO_AAC_MODE_FPM	**FPM AAC Mode** 00: Performing 2-Step AAC 01: Bypassing AAC and Reuse Previous Value 10: Performing Step 1 Only AAC 11: Bypassing AAC and Use Manually Controlled Value
8:7	XO_AAC_MODE_LPM	**LPM AAC Mode** 00: Performing 2-Step AAC 01: Bypassing AAC and Reuse Previous Value 10: Performing Step 1 Only AAC 11: Bypassing AAC and Use Manually Controlled Value
6:5	XO_AAC_FPM_TIME	**AAC FPM Time** 00: 16T 32K Clock Cycle 01: 32T 32K Clock Cycle 10: 64T 32K Clock Cycle 11: 128T 32K Clock Cycle
4	XO_STRUP_MODE	**Start-Up Mode** 0: Open OR Close Detection 1: Open AND Close Detection
3	XO_XMODE_M	**XMODE Manual Control when XO_XMODE_MAN is 1** 0: XMODE = 0 1: XMODE = 1
2	XO_XMODE_MAN	**XMODE Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
1	XO_EN32K_M	**EN_32K Manual Control when XO_EN32K_MAN is 1** 0: EN_32K = 0 1: EN_32K = 1
0	XO_EN32K_MAN	**EN_32K Control Mode** 0: HW-Control Mode

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Bit(s)	Name	Description
		1: Manual-Control Mode

0D2E **DCXO_CW03** **DCXO Code Word 3** **8408**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_FPM_ISEL_MAN					XO_LPM_ISEL_MAN					XO_RESERVED0		XO_BUFLDO13_VSET_M			
Type	RW					RW					RW		RW			
Reset	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
15:11	XO_FPM_ISEL_MAN	**XO Core FPM Current Setting when XO_AAC_MODE_LPM is 2'b11**
10:6	XO_LPM_ISEL_MAN	**XO Core LPM Current Setting when XO_AAC_MODE_FPM is 2'b11**
5:4	XO_RESERVED0	**Reserved Register**
3:0	XO_BUFLDO13_VSET_M	**EXTBUF13 LDO Output Voltage Manual Setting when XO_LDO_MAN is 1**

0D30 **DCXO_CW04** **DCXO Code Word 4** **FF55**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CDAC_LPM								XO_CDAC_FPM							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
15:8	XO_CDAC_LPM	**XO CDAC Code (Complement) during LPM**
7:0	XO_CDAC_FPM	**XO CDAC Code (Complement) during FPM**

0D32 **DCXO_CW05** **DCXO Code Word 5** **DD40**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_COFST_FPM		XO_32KDIV_NFRAC_FPM													
Type	RW		RW													
Reset	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	XO_COFST_FPM	**XO CDAC Offset Code during FPM**
13:0	XO_32KDIV_NFRAC_FPM	**32K Clock Divider Fraction Setting during FPM**

0D34 **DCXO_CW06** **DCXO Code Word 6** **2318**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_COFST_LPM		XO_32KDIV_NFRAC_LPM													
Type	RW		RW													
Reset	0	0	1	0	0	0	1	1	0	0	0	1	1	0	0	0

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Bit(s)	Name	Description
15:14	XO_COFST_LPM	**XO CDAC Offset Code during LPM**
13:0	XO_32KDIV_NFRAC_LPM	**32K Clock Divider Fraction Setting during LPM**

0D36 DCXO_CW07 DCXO Code Word 7 8FFE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CORE_IDAC_FPM		XO_CORE_GMX2_FPM	XO_CORE_BYPCAS_FPM	XO_ILPM_COMP_EN_M	XO_IFPM_COMP_EN_M	XO_IAAC_COMP_EN_M	XO_VTCGEN_EN_M	XO_LPMBIAS_EN_M	XO_CORE_VBLPM_EN_M	XO_CORE_VBFPM_EN_M	XO_STARTUP_EN_M	XO_CORE_AAC_EN_M	XO_CORE_TURBO_EN_M	XO_CORE_EN_M	XO_CORE_MAN
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0

Bit(s)	Name	Description
15:14	XO_CORE_IDAC_FPM	**XO Core GM Current Control during FPM or when XO_CORE_MAN is 1**
13	XO_CORE_GMX2_FPM	**XO Core GM Double Option during FPM or when XO_CORE_MAN is 1** 0: DA_XO_CORE_GMX2_SYNC = 0 1: DA_XO_CORE_GMX2_SYNC = 1
12	XO_CORE_BYPCAS_FPM	**XO Core Bypass Cascode Option during FPM or when XO_CORE_MAN is 1** 0: DA_XO_CORE_BYPCAS_SYNC = 0 1: DA_XO_CORE_BYPCAS_SYNC = 1
11	XO_ILPM_COMP_EN_M	**XO ILPM to Comparator Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
10	XO_IFPM_COMP_EN_M	**XO IFPM to Comparator Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
9	XO_IAAC_COMP_EN_M	**XO IAAC to Comparator Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
8	XO_VTCGEN_EN_M	**FPM GM Bias Circuit Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
7	XO_LPMBIAS_EN_M	**XO core LPM Bias Circuit Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
6	XO_CORE_VBLPM_EN_M	**XO Core LPM Bias Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
5	XO_CORE_VBFPM_EN_M	**XO Core FPM Bias Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
4	XO_STARTUP_EN_	**XO Core Start-Up Gating Manual Control when XO_CORE_MAN is**

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Bit(s)	Name	Description
	M	**1** 0: Disabled 1: Enabled
3	XO_CORE_AAC_EN_M	**XO Core AAC Bias Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
2	XO_CORE_TURBO_EN_M	**XO Core ITurbo Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
1	XO_CORE_EN_M	**XO Core Oscillator Manual Control when XO_CORE_MAN is 1** 0: Disabled 1: Enabled
0	XO_CORE_MAN	**XO Core Control Mode** 0: HW-Control Mode 1: Manual-Control Mode

0D38 DCXO_CW08 DCXO Code Word 8 46BE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_AAC_COMP_POL	XO_AAC_VSEL_FPM				XO_AAC_COMP_HV_FPM	XO_AAC_VOFST_FPM		XO_AAC_IBIAS_FPM		XO_AAC_HV_FPM	XO_COMP_TSTEN_M	XO_COMP_EN_M	XO_AAC_MONEN_M	XO_AAC_EN_M	XO_AAC_COMP_MAN
Type	RW	RW				RW	RW		RW		RW	RW	RW	RW	RW	RW
Reset	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	0

Bit(s)	Name	Description
15	XO_AAC_COMP_POL	**Polarity of AD_XO_AAC_COMP_OUT** 0: Normal 1: Inverted
14:11	XO_AAC_VSEL_FPM	**XO AAC Target Peak-to-Peak Amplitude during FPM or when XO_AAC_COMP_MAN is 1**
10	XO_AAC_COMP_HV_FPM	**XO AAC COMP High Amplitude Mode during FPM or when XO_AAC_COMP_MAN is 1**
9:8	XO_AAC_VOFST_FPM	**XO AAC Input Offset Settings during FPM or XO_AAC_COMP_MAN=1**
7:6	XO_AAC_IBIAS_FPM	**XO AAC Bias Current Setting during FPM or when XO_AAC_COMP_MAN is 1**
5	XO_AAC_HV_FPM	**XO AAC High Amplitude Mode during FPM or when XO_AAC_COMP_MAN is 1**
4	XO_COMP_TSTEN_M	**XO COMP Voltage Testing Mode Manual Control during Start-Up or when XO_AAC_COMP_MAN is 1** 0: Disabled 1: Enabled
3	XO_COMP_EN_M	**XO COMP Manual Control during AAC or when XO_AAC_COMP_MAN is 1** 0: Disabled 1: Enabled
2	XO_AAC_MONEN_M	**XO AAC Voltage Monitor Manual Control during Start-Up or when XO_AAC_COMP_MAN is 1** 0: Disabled 1: Enabled

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Bit(s)	Name	Description
1	XO_AAC_EN_M	**XO Core AAC Manual Control during AAC or when XO_AAC_COMP_MAN is 1** 0: Disabled 1: Enabled
0	XO_AAC_COMP_MAN	**XO AAC COMP Control Mode** 0: HW-Control Mode 1: Manual-Control Mode

0D3A **DCXO_CW09** **DCXO Code Word 9** **00CF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_SWRST	XO_AAC_FPM_SWEN	XO_AAC_VOFST_LPM		XO_AAC_IBIAS_LPM		XO_AAC_HV_LPM	XO_AAC_VSEL_LPM				XO_AAC_COMP_HV_LPM	XO_CORE_IDAC_LPM		XO_CORE_GMX2_LPM	XO_CORE_BYPCAS_LPM
Type	RW	RW	RW		RW		RW	RW				RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1

Bit(s)	Name	Description
15	XO_SWRST	**XO Digital Macro Software Reset** 0: Normal 1: Reset
14	XO_AAC_FPM_SWEN	**SW-Triggered AAC Control during FPM** 0: Disabled 1: Enabled
13:12	XO_AAC_VOFST_LPM	**XO AAC Input Offset Setting during LPM**
11:10	XO_AAC_IBIAS_LPM	**XO AAC Bias Current Setting during LPM**
9	XO_AAC_HV_LPM	**XO AAC High Amplitude Mode during LPM**
8:5	XO_AAC_VSEL_LPM	**XO AAC Target Peak-to-Peak Amplitude during LPM**
4	XO_AAC_COMP_HV_LPM	**XO AAC COMP High Amplitude Mode during LPM**
3:2	XO_CORE_IDAC_LPM	**XO GM Core Current Control during LPM**
1	XO_CORE_GMX2_LPM	**XO Core GM Double Option during LPM**
0	XO_CORE_BYPCAS_LPM	**XO Core Bypass Cascode Option during LPM**

0D3C **DCXO_CW10** **DCXO Code Word 10** **EF50**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_VBIST_EN_M	XO_TEST_VCAL_EN_M	XO_LDOVTST_EN_M	XO_LDOPBUF_VSET_M				XO_LDOPBUF_EN_M	XO_LDO_MAN	XO_CTL_SYNC_EN_M	XO_CTL_SYNC_MAN	XO_CBANK_SYNC_EN_M	XO_CBANK_SYNC_MAN	XO_32KDIV_TEST_EN	XO_32KDIV_RATIO_MAN	XO_32KDIV_SWRST
Type	RW	RW	RW	RW				RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	0	1	1	1	1	0	1	0	1	0	0	0	0

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Bit(s)	Name	Description
15	XO_VBIST_EN_M	**XO self Voltage Calibration Monitor Path Manual Control when XO_LDO_MAN is 1** 0: Disabled 1: Enabled
14	XO_TEST_VCAL_EN_M	**XO Self Voltage Calibrated Mode Manual Control when XO_LDO_MAN is 1** 0: Disabled 1: Enabled
13	XO_LDOVTST_EN_M	**XO PBUF LDO Voltage TestMux Manual Control when XO_LDO_MAN is 1** 0: Disabled 1: Enabled
12:9	XO_LDOPBUF_VSET_M	**XO PBUF LDO Output Voltage Manual Setting when XO_LDO_MAN is 1** 0: Disabled 1: Enabled
8	XO_LDOPBUF_EN_M	**XO Internal Buffer Bias Manual Control when XO_LDO_MAN is 1** 0: Disabled 1: Enabled
7	XO_LDO_MAN	**XO LDO Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
6	XO_CTL_SYNC_EN_M	**XO Local CTL Sync Manual Control when XO_CTL_SYNC_MAN is 1** 0: Disabled 1: Enabled
5	XO_CTL_SYNC_MAN	**XO Local CTL Sync Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
4	XO_CBANK_SYNC_EN_M	**XO Local CBANK Sync Manual Control when XO_CBANK_SYNC_MAN is 1** 0: Disabled 1: Enabled
3	XO_CBANK_SYNC_MAN	**XO Local CBANK Sync Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
2	XO_32KDIV_TEST_EN	**32K Clock Divider Testing Output Control through DCXO_AUXOUT** 0: Disabled 1: Enabled
1	XO_32KDIV_RATIO_MAN	**32K Clock Divider Ratio Control Mode** 0: HW-Control Mode 1: 32KDIV_RATIO = 1
0	XO_32KDIV_SWRST	**32K Clock Divider Software Reset** 0: Normal 1: Reset

0D3E **DCXO_CW11** **DCXO Code Word 11** **8A60**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_LDOPBUF_ENCL	RG_XO_LDOPBUF_BYP	RG_XO_LPBUF_INV	RG_XO_CTL_SYNC_BYP	RG_XO_CTL_POL	RG_XO_CBANK_SYNC_BYP	RG_XO_CBANK_POL	RG_XO_SYNC_CKPOL	RG_XO_THADC_EN	RG_XO_CORE_OSCTD		XO_VTEST_SEL_MUX				

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Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW				
Reset	1	0	0	0	1	0	1	0	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
15	RG_XO_LDOPBUF_ENCL	**XO Control Signal of XO PBUFLDO Closed Loop** 0: Disabled 1: Enabled
14	RG_XO_LDOPBUF_BYP	**XO Control Signal of XO PBUFLDO Bypass Mode** 0: No Bypassing 1: Bypassing
13	RG_XO_LPBUF_INV	**XO Control Signal of Clock Inversion for Low Power Buffer Chain** 0: Normal 1: Inverted
12	RG_XO_CTL_SYNC_BYP	**XO Control Signal for Bypassing Bias Control Local Synchronization** 0: No Bypassing 1: Bypassing
11	RG_XO_CTL_POL	**XO Control Signal of Clock Polarity for Bias Control Local Synchronization** 0: Postive Edge 1: Negative Edge
10	RG_XO_CBANK_SYNC_BYP	**XO Control Signal for Bypassing CBANK Control Local Synchronization** 0: No Bypassing 1: Bypassing
9	RG_XO_CBANK_POL	**XO Control Signal of Clock Polarity for CBANK Control Local Synchronization** 0: Postive Edge 1: Negative Edge
8	RG_XO_SYNC_CKPOL	**XO Control Signal of Local Synchronized Clock Polarity** 0: In-Phase of X1 1: Out-of-Phase of X1
7	RG_XO_THADC_EN	**XO Control Signal of Vbe Monitoring by AUXADC, for XO Temperature Sensing**
6:5	RG_XO_CORE_OSCTD	**XO Control Signal of Start-Up Delay (Open-Loop)**
4:0	XO_VTEST_SEL_MUX	**XO TestMux Selection**

0D40 **DCXO_CW12** **DCXO Code Word 12** **8F6A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_BUFLDO24_VSET_M				RG_XO_BUFLDO24_IBX2	RG_XO_BUFLDO24_ENCL	XO_RESERVED1	RG_XO_BUFLDO13_IX2	RG_XO_BUFLDO13_IBX2	RG_XO_BUFLDO13_ENCL	RG_XO_IBUF_ISET		RG_XO_PBUF_ISET		RG_XO_VGBIAS_VSET	
Type	RW				RW	RW	RW	RW	RW	RW	RW		RW		RW	
Reset	1	0	0	0	1	1	1	1	0	1	1	0	1	0	1	0

Bit(s)	Name	Description
15:12	XO_BUFLDO24_VSET_M	**EXTBUF13 LDO Output Voltage Manual Setting when XO_LDO_MAN is 1**

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Bit(s)	Name	Description
11	RG_XO_BUFLDO24_IBX2	**XO Control Signal of Bias Current Doubler on EXTBUF24 LDO**
10	RG_XO_BUFLDO24_ENCL	**XO Control Signal of EXTBUF24 LDO Closed Loop** 0: Disabled 1: Enabled
9	XO_RESERVED1	**Reserved Register**
8	RG_XO_BUFLDO13_IX2	**XO Control Signal of Double Current on EXTBUF13 LDO**
7	RG_XO_BUFLDO13_IBX2	**XO Control Signal of Bias Current Doubler on EXTBUF13 LDO**
6	RG_XO_BUFLDO13_ENCL	**XO Control Signal of EXTBUF13 LDO Closed Loop** 0: Disabled 1: Enabled
5:4	RG_XO_IBUF_ISET	**XO Control Signal of Internal Isolated Buffer Current**
3:2	RG_XO_PBUF_ISET	**XO Control Signal of FPM Pre-buffer Current**
1:0	RG_XO_VGBIAS_VSET	**XO Control Signal of XO Input Gate Bias during FPM**

0D42 **DCXO_CW13** **DCXO Code Word 13** **AAAA**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_XO_EXTBUF4_ISET		RG_XO_EXTBUF4_HD		RG_XO_EXTBUF3_ISET		RG_XO_EXTBUF3_HD		RG_XO_EXTBUF2_ISET		RG_XO_EXTBUF2_HD		RG_XO_EXTBUF1_ISET		RG_XO_EXTBUF1_HD	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
15:14	RG_XO_EXTBUF4_ISET	**XO Control Signal of Current on EXTBUF4**
13:12	RG_XO_EXTBUF4_HD	**XO Control Signal of EXTBUF4 Output Driving Strength**
11:10	RG_XO_EXTBUF3_ISET	**XO Control Signal of Current on EXTBUF3**
9:8	RG_XO_EXTBUF3_HD	**XO Control Signal of EXTBUF3 Output Driving Strength**
7:6	RG_XO_EXTBUF2_ISET	**XO Control Signal of Current on EXTBUF2**
5:4	RG_XO_EXTBUF2_HD	**XO Control Signal of EXTBUF2 Output Driving Strength**
3:2	RG_XO_EXTBUF1_ISET	**XO Control Signal of Current on EXTBUF1**
1:0	RG_XO_EXTBUF1_HD	**XO Control Signal of EXTBUF1 Output Driving Strength**

0D44 **DCXO_CW14** **DCXO Code Word 14** **BC2A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_CAL_E	XO_CAL_E	RG_XO_RESERVED1			XO_VIO18P	RG_XO_RESERVED0			XO_EXTBU	RG_XO_AUDIO_ISET		RG_XO_AUDIO_ATTE		RG_XO_LPM_PREBUF	

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	N_M	N_M AN				G_BU FEN				F4_C LKSE L_MA N			N		_ISET	
Type	RW	RW	RW			RW	RW			RW	RW		RW		RW	
Reset	1	0	1	1	1	1	0	0	0	0	1	0	1	0	1	0

Bit(s)	Name	Description
15	XO_CAL_EN_M	**CAL_EN Manual Control when XO_CAL_EN_MAN is 1** 0: CAL_EN = 0 1: CAL_EN = 1
14	XO_CAL_EN_MAN	**CAL_EN Control Mode** 0: HW-Control Mode 1: Manual-Control Mode
13:11	RG_XO_RESERVED1	**Reserved Register**
10	XO_VIO18PG_BUFEN	**Clock Buffer Enable Signal Gating Control** 0: Not Gated by VIO18_PG 1: Gated by VIO18_PG
9:7	RG_XO_RESERVED0	**Reserved Register**
6	XO_EXTBUF4_CLKSEL_MAN	**XO_CEL Clock Buffer Enable Control Mode** 0: Pin-Control Mode 1: Register-Control Mode
5:4	RG_XO_AUDIO_ISET	**XO Control Signal of Audio Buffer Current**
3:2	RG_XO_AUDIO_ATTEN	**XO Control Signal of RC Filter on Audio Path**
1:0	RG_XO_LPM_PREBUF_ISET	**XO Control Signal of Current for 26MHz Low-Power Pre-buffer**

0D46 DCXO_CW15 DCXO Code Word 15 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_AUXOUT_SEL										XO_STATIC_AUXOUT_SEL					
Type	RW										RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:6	XO_AUXOUT_SEL	**Dynamic AuxOut Selection**
5:0	XO_STATIC_AUXOUT_SEL	**Static AuxOut Selection**

0D48 DCXO_CW16 DCXO Code Word 16 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XO_STATIC_AUXOUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	XO_STATIC_AUXOUT	**Static AuxOut**

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0E00 AUXADC_ADC_0 AUXADC ADC register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0	AUXADC_ADC_OUT_CH0														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0	**AUXADC channel 0 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0	**AUXADC channel 0 output data**

0E02 AUXADC_ADC_1 AUXADC ADC register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1	AUXADC_ADC_OUT_CH1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1	**AUXADC channel 1 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1	**AUXADC channel 1 output data**

0E04 AUXADC_ADC_2 AUXADC ADC register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH2				AUXADC_ADC_OUT_CH2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY	**AUXADC channel 2 output data ready**

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Bit(s)	Name	Description
	_CH2	0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH2	**AUXADC channel 2 output data**

0E06 **AUXADC_ADC3** **AUXADC ADC register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH3				AUXADC_ADC_OUT_CH3											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH3	**AUXADC channel 3 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH3	**AUXADC channel 3 output data**

0E08 **AUXADC_ADC4** **AUXADC ADC register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4				AUXADC_ADC_OUT_CH4											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4	**AUXADC channel 4 output data**

0E0A **AUXADC_ADC5** **AUXADC ADC register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH5				AUXADC_ADC_OUT_CH5											

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Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH5	**AUXADC channel 5 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH5	**AUXADC channel 5 output data**

0E0C **AUXADC_ADC6** AUXADC ADC register 6 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH6**				**AUXADC_ADC_OUT_CH6**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH6	**AUXADC channel 6 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH6	**AUXADC channel 6 output data**

0E0E **AUXADC_ADC7** AUXADC ADC register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH7**	**AUXADC_ADC_OUT_CH7**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7	**AUXADC channel 7 output data**

0E10 **AUXADC_ADC8** AUXADC ADC register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**AUXADC_ADC_RDY_CH8**				**AUXADC_ADC_OUT_CH8**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH8	**AUXADC channel 8 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH8	**AUXADC channel 8 output data**

0E12 **AUXADC_ADC9** **AUXADC ADC register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH9**				**AUXADC_ADC_OUT_CH9**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH9	**AUXADC channel 9 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH9	**AUXADC channel 9 output data**

0E14 **AUXADC_ADC10** **AUXADC ADC register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH10**				**AUXADC_ADC_OUT_CH10**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH10	**AUXADC channel 10 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH10	**AUXADC channel 10 output data**

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0E16 **AUXADC_ADC_11** **AUXADC ADC register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH11				AUXADC_ADC_OUT_CH11											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH11	**AUXADC channel 11 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH11	**AUXADC channel 11 output data**

0E18 **AUXADC_ADC_12** **AUXADC ADC register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH12_15				AUXADC_ADC_OUT_CH12_15											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH12_15	**AUXADC channel 12_15 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH12_15	**AUXADC channel 12_15 output data**

0E1A **AUXADC_ADC_13** **AUXADC ADC register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_THR_HW				AUXADC_ADC_OUT_THR_HW											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_THR_HW	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding

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Bit(s)	Name	Description
		1: AUXADC data ready
11:0	AUXADC_ADC_OUT_THR_HW	**AUXADC channel 4 output data**

0E1C **AUXADC_ADC_14** **AUXADC ADC register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_LBAT				AUXADC_ADC_OUT_LBAT											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT	**AUXADC low battery output data**

0E1E **AUXADC_ADC_15** **AUXADC ADC register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_LBAT2				AUXADC_ADC_OUT_LBAT2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT2	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT2	**AUXADC low battery output data**

0E20 **AUXADC_ADC_16** **AUXADC ADC register 16** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_	AUXADC_ADC_OUT_CH7_BY_GPS														

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	BY_GPS															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_GPS	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_GPS	**AUXADC channel 7 output data**

0E22 **AUXADC_ADC_17** **AUXADC ADC register 17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_MD	AUXADC_ADC_OUT_CH7_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_MD	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_MD	**AUXADC channel 7 output data**

0E24 **AUXADC_ADC_18** **AUXADC ADC register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_AP	AUXADC_ADC_OUT_CH7_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_AP	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_AP	**AUXADC channel 7 output data**

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0E26 **AUXADC_ADC_19** **AUXADC ADC register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4_BY_MD				AUXADC_ADC_OUT_CH4_BY_MD											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_MD	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_MD	**AUXADC channel 4 output data**

0E28 **AUXADC_ADC_20** **AUXADC ADC register 20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_PCHR	AUXADC_ADC_OUT_WAKEUP_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_PCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_PCHR	**AUXADC wakeup output data**

0E2A **AUXADC_ADC_21** **AUXADC ADC register 21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_SWCHR	AUXADC_ADC_OUT_WAKEUP_SWCHR														
Type	RO	RO														

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_SWCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_SWCHR	**AUXADC wakeup output data**

0E2C **AUXADC_ADC_22** **AUXADC ADC register 22** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_MD	AUXADC_ADC_OUT_CH0_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_MD	**AUXADC channel output data**

0E2E **AUXADC_ADC_23** **AUXADC ADC register 23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_AP	AUXADC_ADC_OUT_CH0_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_AP	**AUXADC channel output data**

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0E30 **AUXADC_ADC_24** **AUXADC ADC register 24** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_MD	AUXADC_ADC_OUT_CH1_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_MD	**AUXADC channel output data**

0E32 **AUXADC_ADC_25** **AUXADC ADC register 25** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_AP	AUXADC_ADC_OUT_CH1_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_AP	**AUXADC channel output data**

0E34 **AUXADC_ADC_26** **AUXADC ADC register 26** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_VISMPS0				AUXADC_ADC_OUT_VISMPS0											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_VISMPS0	**AUXADC vismps output data ready** 0: AUXADC vismps data proceeding 1: AUXADC vismps data ready
11:0	AUXADC_ADC_OUT_VISMPS0	**AUXADC vismps output data**

0E36 **AUXADC_ADC_27** **AUXADC ADC register 27** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC1	AUXADC_ADC_OUT_FGADC1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC1	**AUXADC output data ready (BATSNS)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC1	**AUXADC output data**

0E38 **AUXADC_ADC_28** **AUXADC ADC register 28** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC2	AUXADC_ADC_OUT_FGADC2														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC2	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC2	**AUXADC output data**

0E3A **AUXADC_ADC_29** **AUXADC ADC register 29** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_	AUXADC_ADC_OUT_IMP														

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	ADC_ RDY_ IMP															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP	**AUXADC output data**

0E3C **AUXADC_ADC_30** **AUXADC ADC register 30** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ ADC_ RDY_ IMP_ AVG	AUXADC_ADC_OUT_IMP_AVG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP_AVG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP_AVG	**AUXADC output data**

0E3E **AUXADC_ADC_31** **AUXADC ADC register 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXADC_ADC_OUT_RAW														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	AUXADC_ADC_OUT_RAW	**AUXADC channel output raw data**

0E40 **AUXADC_ADC_32** **AUXADC ADC register 32** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ ADC_	AUXADC_ADC_OUT_MDRT														

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	RDY_MDRT															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDRT	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_MDRT	**AUXADC output data**

0E42 **AUXADC_ADC_33** **AUXADC ADC register 33** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_MDBG	AUXADC_ADC_OUT_MDBG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDBG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_MDBG	**AUXADC output data**

0E44 **AUXADC_ADC_34** **AUXADC ADC register 34** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_DCXO_BY_GPS				AUXADC_ADC_OUT_DCXO_BY_GPS											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_DCXO_BY_GPS	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_DCXO_BY_GPS	**AUXADC channel 4 output data**

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0E46 **AUXADC_ADC_35** **AUXADC ADC register 35** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_DCXO_BY_MD				AUXADC_ADC_OUT_DCXO_BY_MD											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_DCXO_BY_MD	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_DCXO_BY_MD	**AUXADC channel 4 output data**

0E48 **AUXADC_ADC_36** **AUXADC ADC register 36** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_DCXO_BY_AP				AUXADC_ADC_OUT_DCXO_BY_AP											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_DCXO_BY_AP	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_DCXO_BY_AP	**AUXADC channel 4 output data**

0E4A **AUXADC_ADC_37** **AUXADC ADC register 37** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_DCXO_MDRT				AUXADC_ADC_OUT_DCXO_MDRT											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_DCXO_MDRT	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_DCXO_MDRT	**AUXADC output data**

0E4C AUXADC_ADC_38 AUXADC ADC register 38 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_NAG	AUXADC_ADC_OUT_NAG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_NAG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_NAG	**AUXADC output data**

0E4E AUXADC_ADC_39 AUXADC ADC register 39 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_TYPEC_H				AUXADC_ADC_OUT_TYPEC_H											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_TYPEC_H	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_TYPEC_H	**AUXADC low battery output data**

0E50 AUXADC_ADC_40 AUXADC ADC register 40 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX				AUXADC_ADC_OUT_TYPEC_L											

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	ADC_ ADC_ RDY_ TYPE C_L															
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_TYPEC_L	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_TYPEC_L	**AUXADC low battery output data**

0E52 **AUXADC_BUF0** **AUXADC_BUF0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ BUF_ RDY_ 00	AUXADC_BUF_OUT_00														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_00	**AUXADC_BUF_00** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_00	

0E54 **AUXADC_BUF1** **AUXADC_BUF1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUX ADC_ BUF_ RDY_ 01	AUXADC_BUF_OUT_01														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_01	**AUXADC_BUF_01** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_01	

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0E56 **AUXADC_BUF2** **AUXADC_BUF2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_02	AUXADC_BUF_OUT_02														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_02	**AUXADC_BUF_02** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_02	

0E58 **AUXADC_BUF3** **AUXADC_BUF3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_03	AUXADC_BUF_OUT_03														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_03	**AUXADC_BUF_03** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_03	

0E5A **AUXADC_BUF4** **AUXADC_BUF4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_04	AUXADC_BUF_OUT_04														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_04	**AUXADC_BUF_04** 0: AUXADC data proceeding 1: AUXADC data ready

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Bit(s)	Name	Description
14:0	AUXADC_BUF_OUT_04	

0E5C **AUXADC_BUF5** **AUXADC_BUF5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_05	AUXADC_BUF_OUT_05														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_05	**AUXADC_BUF_05** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_05	

0E5E **AUXADC_BUF6** **AUXADC_BUF6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_06	AUXADC_BUF_OUT_06														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_06	**AUXADC_BUF_06** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_06	

0E60 **AUXADC_BUF7** **AUXADC_BUF7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_07	AUXADC_BUF_OUT_07														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_BUF_RDY_07	**AUXADC_BUF_07** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_07	

0E62 **AUXADC_BUF8** **AUXADC_BUF8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_08	AUXADC_BUF_OUT_08														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_08	**AUXADC_BUF_08** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_08	

0E64 **AUXADC_BUF9** **AUXADC_BUF9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_09	AUXADC_BUF_OUT_09														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_09	**AUXADC_BUF_09** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_09	

0E66 **AUXADC_BUF10** **AUXADC_BUF10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_	AUXADC_BUF_OUT_10														

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	BUF_ RDY_ 10															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_10	**AUXADC_BUF_10** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_10	

0E68 AUXADC_BUF11 AUXADC_BUF11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_11	AUXADC_BUF_OUT_11														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_11	**AUXADC_BUF_11** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_11	

0E6A AUXADC_BUF12 AUXADC_BUF12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_12	AUXADC_BUF_OUT_12														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_12	**AUXADC_BUF_12** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_12	

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0E6C **AUXADC_BUF_13** **AUXADC_BUF13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_13	AUXADC_BUF_OUT_13														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_13	**AUXADC_BUF_13** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_13	

0E6E **AUXADC_BUF_14** **AUXADC_BUF14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_14	AUXADC_BUF_OUT_14														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_14	**AUXADC_BUF_14** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_14	

0E70 **AUXADC_BUF_15** **AUXADC_BUF15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_15	AUXADC_BUF_OUT_15														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_15	**AUXADC_BUF_15** 0: AUXADC data proceeding 1: AUXADC data ready

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Bit(s)	Name	Description
14:0	AUXADC_BUF_OUT_15	

0E72 AUXADC_BUF16 AUXADC_BUF16 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_16	AUXADC_BUF_OUT_16														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_16	**AUXADC_BUF_16** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_16	

0E74 AUXADC_BUF17 AUXADC_BUF17 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_17	AUXADC_BUF_OUT_17														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_17	**AUXADC_BUF_17** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_17	

0E76 AUXADC_BUF18 AUXADC_BUF18 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_18	AUXADC_BUF_OUT_18														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_BUF_RDY_18	**AUXADC_BUF_18** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_18	

0E78 **AUXADC_BUF19** **AUXADC_BUF19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_19	AUXADC_BUF_OUT_19														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_19	**AUXADC_BUF_19** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_19	

0E7A **AUXADC_BUF20** **AUXADC_BUF20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_20	AUXADC_BUF_OUT_20														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_20	**AUXADC_BUF_20** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_20	

0E7C **AUXADC_BUF21** **AUXADC_BUF21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_	AUXADC_BUF_OUT_21														

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	BUF_ RDY_ 21															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_21	**AUXADC_BUF_21** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_21	

0E7E **AUXADC_BUF22** AUXADC_BUF22 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_22**	**AUXADC_BUF_OUT_22**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_22	**AUXADC_BUF_22** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_22	

0E80 **AUXADC_BUF23** AUXADC_BUF23 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_23**	**AUXADC_BUF_OUT_23**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_23	**AUXADC_BUF_23** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_23	

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0E82 **AUXADC_BUF_24** **AUXADC_BUF24** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_24	AUXADC_BUF_OUT_24														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_24	**AUXADC_BUF_24** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_24	

0E84 **AUXADC_BUF_25** **AUXADC_BUF25** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_25	AUXADC_BUF_OUT_25														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_25	**AUXADC_BUF_25** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_25	

0E86 **AUXADC_BUF_26** **AUXADC_BUF26** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_26	AUXADC_BUF_OUT_26														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_26	**AUXADC_BUF_26** 0: AUXADC data proceeding 1: AUXADC data ready

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Bit(s)	Name	Description
14:0	AUXADC_BUF_OUT_26	

0E88 **AUXADC_BUF27** **AUXADC_BUF27** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_27	AUXADC_BUF_OUT_27														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_27	**AUXADC_BUF_27** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_27	

0E8A **AUXADC_BUF28** **AUXADC_BUF28** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_28	AUXADC_BUF_OUT_28														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_28	**AUXADC_BUF_28** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_28	

0E8C **AUXADC_BUF29** **AUXADC_BUF29** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_29	AUXADC_BUF_OUT_29														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_BUF_RDY_29	**AUXADC_BUF_29** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_29	

0E8E **AUXADC_BUF30** **AUXADC_BUF30** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_30	AUXADC_BUF_OUT_30														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_30	**AUXADC_BUF_30** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_30	

0E90 **AUXADC_BUF31** **AUXADC_BUF31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_31	AUXADC_BUF_OUT_31														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_31	**AUXADC_BUF_31** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_31	

0E92 **AUXADC_STA0** **AUXADC_STA0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_	AUXADC_A	AUXADC_A	AUXADC_A	AUXADC_ADC_BUSY_IN											

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	ADC_BUSY_IN_WAKEUP	DC_BUSY_IN_VISMPS0	DC_BUSY_IN_LBAT2	DC_BUSY_IN_LBAT												
Type	RO	RO	RO	RO	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_WAKEUP	**ADC busy status** 1: BUSY 0: IDLE
14	AUXADC_ADC_BUSY_IN_VISMPS0	**ADC busy status** 1: BUSY 0: IDLE
13	AUXADC_ADC_BUSY_IN_LBAT2	**ADC busy status** 1: BUSY 0: IDLE
12	AUXADC_ADC_BUSY_IN_LBAT	**ADC busy status** 1: BUSY 0: IDLE
11:0	AUXADC_ADC_BUSY_IN	**AUXADC ADC BUSY STATUS, bit[11] = CH11 ~ bit[0] = CH0** 1 : BUSY 0 : IDLE

0E94 **AUXADC_STA1** **AUXADC_STA1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_THR_MD	AUXADC_ADC_BUSY_IN_THR_HW	AUXADC_ADC_BUSY_IN_GPS	AUXADC_ADC_BUSY_IN_GPS_MD	AUXADC_ADC_BUSY_IN_GPS_AP	AUXADC_ADC_BUSY_IN_FGADC2	AUXADC_ADC_BUSY_IN_FGADC1	AUXADC_ADC_BUSY_IN_IMP	AUXADC_ADC_BUSY_IN_SHARE	AUXADC_ADC_BUSY_IN_MDBG	AUXADC_ADC_BUSY_IN_MDRT		AUXADC_ADC_BUSY_IN_DCXO_GPS	AUXADC_ADC_BUSY_IN_DCXO_GPS_MD	AUXADC_ADC_BUSY_IN_DCXO_GPS_AP	AUXADC_ADC_BUSY_IN_DCXO_MDRT
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_THR_MD	**ADC busy status** 1: BUSY 0: IDLE
14	AUXADC_ADC_BUSY_IN_THR_HW	**ADC busy status** 1: BUSY 0: IDLE
13	AUXADC_ADC_BUSY_IN_GPS	**ADC busy status** 1: BUSY 0: IDLE
12	AUXADC_ADC_BUSY_IN_GPS_MD	**ADC busy status** 1: BUSY 0: IDLE
11	AUXADC_ADC_BUSY_IN_GPS_AP	**ADC busy status** 1: BUSY

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Bit(s)	Name	Description
		0: IDLE
10	AUXADC_ADC_BUSY_IN_FGADC2	**ADC busy status** 1: BUSY 0: IDLE
9	AUXADC_ADC_BUSY_IN_FGADC1	**ADC busy status** 1: BUSY 0: IDLE
8	AUXADC_ADC_BUSY_IN_IMP	**ADC busy status** 1: BUSY 0: IDLE
7	AUXADC_ADC_BUSY_IN_SHARE	**ADC busy status** 1: BUSY 0: IDLE
6	AUXADC_ADC_BUSY_IN_MDBG	**ADC busy status** 1: BUSY 0: IDLE
5	AUXADC_ADC_BUSY_IN_MDRT	**ADC busy status** 1: BUSY 0: IDLE
3	AUXADC_ADC_BUSY_IN_DCXO_GPS	**ADC busy status** 1: BUSY 0: IDLE
2	AUXADC_ADC_BUSY_IN_DCXO_GPS_MD	**ADC busy status** 1: BUSY 0: IDLE
1	AUXADC_ADC_BUSY_IN_DCXO_GPS_AP	**ADC busy status** 1: BUSY 0: IDLE
0	AUXADC_ADC_BUSY_IN_DCXO_MDRT	**ADC busy status** 1: BUSY 0: IDLE

0E96 **AUXADC_STA2** **AUXADC_STA2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_NAG	AUXADC_ADC_BUSY_IN_TYPEC_L	AUXADC_ADC_BUSY_IN_TYPEC_H													
Type	RO	RO	RO													
Reset	0	0	0													

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_NAG	**ADC busy status** 1: BUSY 0: IDLE
14	AUXADC_ADC_BUSY_IN_TYPEC_L	**ADC busy status** 1: BUSY

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Bit(s)	Name	Description
		0: IDLE
13	AUXADC_ADC_BUSY_IN_TYPEC_H	**ADC busy status** 1: BUSY 0: IDLE

0EC0 **AUXADC_CON12** **AUXADC_CON12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VBE_SEL	RG_VBUF_EN											
Type				RW	RW											
Reset				0	0											

Bit(s)	Name	Description
12	RG_VBE_SEL	**1: DCXO buffer / 0: PMIC buffer**
11	RG_VBUF_EN	**1: turn on Vbuf. / 0: turn off Vbuf.**

0F58 **ACCDET_CON0** **ACCDET control register 0** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_AUDACCDETMICBIAS0PULLLOW	AUDACCDETAUXADCSWCTRL_SEL		RG_AUDACCDETVIN1PULLLOW	RG_AUDACCDETTVDET	RG_AUDACCDETMICBIAS1PULLLOW	RG_AUDACCDETSWCTRL			RG_ACCDETSEL	RG_AUDACCDETANASWCTRLENB	RG_AUDACCDETVTHACAL	RG_AUDACCDETVTHBCAL
Type				RW	RW		RW	RW	RW	RW			RW	RW	RW	RW
Reset				0	0		0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
12	RG_AUDACCDETMICBIAS0PULLLOW	**Pulls low MIC Bias 0 pads when MICBIAS is off** 1'b0: Disable 1'b1: Enable
11	AUDACCDETAUXADCSWCTRL_SEL	1'b0: HW mode 1'b1: SW mode
9	RG_AUDACCDETVIN1PULLLOW	**Pulls low VIN1 pads when MICBIAS is off** 1'b0: Disable 1'b1: Enable
8	RG_AUDACCDETTVDET	**Places audio accessory detection into TV mode**
7	RG_AUDACCDETMICBIAS1PULLLOW	**Pulls low MIC Bias 1 pads when MICBIAS is off** 1'b0: Disable 1'b1: Enable
6:4	RG_AUDACCDETSWCTRL	**Controls ACCDET to AUXADC switch** 001: Normal mode 010: 200K 100: 100K Others: Not allowed

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Bit(s)	Name	Description
3	RG_ACCDETSEL	**Selects ACCDET input** 1'b0: ACCDET pin 1'b1: MICP pin
2	RG_AUDACCDETANASWCTRLENB	
1	RG_AUDACCDETVTHACAL	**Calibrates audio accessory detection voltage threshold A**
0	RG_AUDACCDETVTHBCAL	**Calibrates audio accessory detection voltage threshold B**

0F5A **<u>ACCDET_CON1</u>** **ACCDET control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**accdet_anaswctrl_sel**	**ACCDET_NEGVDET_EN_CTRL**	**ACCDET_NEGVDET_EN**	**ACCDET_EINT_SEQ_INIT**	**ACCDET_EINTDET_EN**	**ACCDET_SEQ_INIT**	**ACCDET_EN**
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	accdet_anaswctrl_sel	**select who control the connection between auxadc and accdet when in hook-key status** 1'b0: auxadc 1'b1: accdet
5	ACCDET_NEGVDET_EN_CTRL	**initialize the status default value** 1'b0: HW mode 1'b1: SW mode
4	ACCDET_NEGVDET_EN	**Enable negative debounce** 1'b0: Disable 1'b1: Enable
3	ACCDET_EINT_SEQ_INIT	**initialize the EINT status default value** 1'b0: Disable 1'b1: Enable
2	ACCDET_EINTDET_EN	**Enable EINT detection** 1'b0: Disable 1'b1: Enable
1	ACCDET_SEQ_INIT	**initialize the ACCDET status default value** 1'b0: normal mode 1'b1: initialized mode
0	ACCDET_EN	**Enables ACCDET** Must be set to 0 before switching to TV mode 1'b0: Disable 1'b1: Enable

0F5C **<u>ACCDET_CON2</u>** **ACCDET control register 2** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ACCDET_EINT_PWM_EN	ACCDET_MBIAS_PWM_EN	ACCDET_VTH_PWM_EN	ACCDET_CMP_PWM_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	ACCDET_EINT_PWM_EN	**Enables PWM of ACCDET EINT unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
2	ACCDET_MBIAS_PWM_EN	**Enables PWM of ACCDET MBIAS unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
1	ACCDET_VTH_PWM_EN	**Enables PWM of ACCDET voltage threshold unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
0	ACCDET_CMP_PWM_EN	**Enables PWM of ACCDET comparator** 1'b0: Disable 1'b1: Enable

0F5E **ACCDET_CON3** **ACCDET control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_WIDTH	**ACCDET PWM width** PWM output frequency = 32,768/(PWM_WIDTH+1)Hz

0F60 **ACCDET_CON4** **ACCDET control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_THRESH	**ACCDET PWM threshold** PWM output duty cycle = (PWM_THRESH+1) / (PWM_WIDTH+1) PWM output high time = (PWM_THRESH+1) / 32,768 sec

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0F62 ACCDET_CON5 ACCDET control register 5 0101

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_FALL_DELAY	ACCDET_RISE_DELAY														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	ACCDET_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET is disabled, the suitable falling delay cycle is necessary.
14:0	ACCDET_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET is enabled, the suitable rising delay cycle is necessary.

0F64 ACCDET_CON6 ACCDET control register 6 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE0	**De-bounce time control of state 0** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768 Hz in the MIC mode.

0F66 ACCDET_CON7 ACCDET control register 7 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE1	**De-bounce time control of state 1** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock and 32,768 Hz in the MIC mode.

0F68 ACCDET_CON8 ACCDET control register 8 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE2															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE2	**De-bounce time control of state 2** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768 Hz in the MIC mode.

0F6A **ACCDET_CON9** ACCDET control register 9 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE3	**De-bounce time control of state 3** De-bounce time = (DEBOUNCE/freq) sec In the TV mode, freq is bus clock 32,768 Hz in the MIC mode.

0F6C **ACCDET_CON10** ACCDET control register 10 0005

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE4	**De-bounce time to control AUXADC when in state 0**

0F70 **ACCDET_CON12** ACCDET control register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_IRQ_POLARITY					ACCDET_EINT_IRQ_CLR	ACCDET_NEGV_IRQ_CLR	ACCDET_IRQ_CLR						ACCDET_EINT_IRQ	ACCDET_NEGV_IRQ	ACCDET_IRQ
Type	RW					RW	RW	RW						RO	RO	RO
Reset	0					0	0	0						0	0	0

Bit(s)	Name	Description
15	ACCDET_EINT_IRQ_POLARITY	**ACCDET EINT IRQ POLARITY** 1'b0: falling edge 1'b1: rising edge
10	ACCDET_EINT_IRQ_CLR	**Clears ACCDET_EINT interrupt status. When ACCDET_EINT interrupt is asserted, IRQ_CLR must be set to 1 to clear the**

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Bit(s)	Name	Description
		interrupt status. This bit will pause all activities of ACCDET_EINT design until both the interrupt status and IRQ_CLR are cleared.
9	ACCDET_NEGV_IRQ_CLR	**Clears ACCDET_NEGV interrupt status. When ACCDET_NEGV interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_NEGV design until both the interrupt status and IRQ_CLR are cleared.**
8	ACCDET_IRQ_CLR	**Clears ACCDET interrupt status** When ACCDET interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET design until both the interrupt status and IRQ_CLR are cleared.
2	ACCDET_EINT_IRQ	**Clear ACCDET_EINT interrupt status**
1	ACCDET_NEGV_IRQ	**Clear ACCDET_NEGV interrupt status**
0	ACCDET_IRQ	**ACCDET interrupt status** Due to this register is cleared by the hardware, the interrupt edge-sensitive scheme should be adopted for this design.

0F74 **ACCDET_CON14** **ACCDET control register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_AUDACCDETAUXADCSWCTRL	ACCDET_CMP_CLK	ACCDET_VTH_CLK	ACCDET_MBIAS_CLK												
Type	RO	RO	RO	RO												
Reset	0	0	0	0												

Bit(s)	Name	Description
15	DA_AUDACCDETAUXADCSWCTRL	**ACCDET to AUXADC switch control**
14	ACCDET_CMP_CLK	**Comparator turn on control for accessory detection**
13	ACCDET_VTH_CLK	**Threshold voltage turn on for accessory detection**
12	ACCDET_MBIAS_CLK	**Earphone bias voltage turn on for accessory detection**

0F76 **ACCDET_CON15** **ACCDET control register 15** **0061**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ACCDET_EINT_PWM_WIDTH			ACCDET_EINT_PWM_THRESH				ACCDET_EINT_DEBOUNCE						
Type			RW			RW				RW						
Reset			0	0		0	0	0		1	1	0				

Bit(s)	Name	Description
13:12	ACCDET_EINT_PWM_WIDTH	**ACCDET EINT PWM width** 2'b00: 4ms 2'b01: 8ms

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Bit(s)	Name	Description
		2'b10: 16ms 2'b11: 32ms
10:8	ACCDET_EINT_PWM_THRESH	**ACCDET EINT PWM threshold** 3'b000: 0.5ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 8ms 3'b110: 16ms 3'b111: 32ms
6:4	ACCDET_EINT_DEBOUNCE	**ACCDET EINT debounce time** 3'b000: 1ms 3'b001: 2ms 3'b010: 4ms 3'b011: 8ms 3'b100: 16ms 3'b101: 32ms 3'b110: 256ms 3'b111: 512ms

0F78 ACCDET_CON16 ACCDET control register 16 0161

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_PWM_RISE_DELAY										ACCDET_EINT_PWM_FALL_DELAY	ACCDET_NEGV_THRESH				
Type	RW										RW	RW				
Reset	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1

Bit(s)	Name	Description
15:6	ACCDET_EINT_PWM_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET_EINT is enabled, the suitable rising delay cycle is necessary.
5	ACCDET_EINT_PWM_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET_EINT is disabled, the suitable falling delay cycle is necessary.
4:0	ACCDET_NEGV_THRESH	**ACCDET NVG debounce threshold** 5'd0: 1/32 5'd1: 2/32 5'd2: 3/32 5'd3: 4/32 5'dN: (N+1)/32

0F7E ACCDET_CON19 ACCDET control register 19 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_	AD_E	AD_N													

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	NI_EINTCMPEN	INTCMPOUT	VDETECTOUT													
Type	RO	RO	RO													
Reset	0	0	0													

Bit(s)	Name	Description
15	DA_NI_EINTCMPEN	
14	AD_EINTCMPOUT	
13	AD_NVDETECTOUT	

0F8C CHR_CON0 Charger control register 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VCDT_HV_DET		RGS_CHRDET	RG_CHR_EN	RG_CSDAC_EN		RGS_CHR_LDO_DET	RG_VCDT_HV_EN
Type									RO		RO	RW	RW		RO	RW
Reset									0		0	0	0		0	1

Bit(s)	Name	Description
7	RGS_VCDT_HV_DET	**Charger-in high voltage detection (with de-bounce).** 0: charge-in voltage < VCDT_HV_VTH 1:charge-in voltage > VCDT_HV_VTH
5	RGS_CHRDET	**Charger-in detect.** 0: No valid charger detected 1: Valid charger detected
4	RG_CHR_EN	**Charger enable setting, which would gated CSDAC_EN, PCHR_AUTO and HWCV_EN** 0: Charger disabled 1: Charger enabled
3	RG_CSDAC_EN	**CS DAC enable.** 0: CS DAC disabled 1: CS DAC enabled
1	RGS_CHR_LDO_DET	**Charger LDO detection. If not detected, pulse charger cannot work.** 0: Invalid charger LDO 1: Valid charger LDO
0	RG_VCDT_HV_EN	**ChargerIn HV detection function enable (0: disable, 1: enable)**

0F8E CHR_CON1 Charger Control Register 1 00F2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VCDT_HV_VTH				RG_VCDT_LV_VTH			
Type									RW				RW			
Reset									1	1	1	1	0	0	1	0

Bit(s)	Name	Description
7:4	RG_VCDT_HV_VTH	**ChargerIn HV detection threshold, default 4.3/9.5V for VTHL/VTHH** 0000~1000: 4.2V~4.6V with 50mV/step

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Bit(s)	Name	Description
		1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step
3:0	RG_VCDT_LV_VTH	**ChargerIn LV detection threshold, default 4.3/9.5V for VTHL/VTHH** 0000~1000: 4.2V~4.6V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step

0F90 CHR_CON2 Charger Control Register 2 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VBAT_CC_DET	RGS_VBAT_CV_DET	RGS_CS_DET		RG_CS_EN	RG_VBAT_CC_EN	RG_VBAT_CV_EN	
Type									RO	RO	RO		RW	RW	RW	
Reset									0	0	0		0	1	0	

Bit(s)	Name	Description
7	RGS_VBAT_CC_DET	**VBAT voltage detection for CC.** 0: VBAT voltage < VBAT_CC_VTH 1: VBAT voltage > VBAT_CC_VTH
6	RGS_VBAT_CV_DET	**VBAT voltage detection for CV.** 0: VBAT voltage < VBAT_CV_VTH 1: VBAT voltage > VBAT_CV_VTH
5	RGS_CS_DET	**Current sense voltage detection.** 0: CS voltage < CS_VTH 1: CS voltage > CS_VTH
3	RG_CS_EN	**Current sense voltage detection comparator enable.** 0: Disabled 1: Enabled
2	RG_VBAT_CC_EN	**Battery CC detection enable (0: disable, 1: enable)**
1	RG_VBAT_CV_EN	**Battery CV detection enable** 0: Disabled 1: Enabled

0F92 CHR_CON3 Charger Control Register 3 00CD

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VBAT_CC_VTH			RG_VBAT_CV_VTH				
Type									RW			RW				
Reset									1	1		0	1	1	0	1

Bit(s)	Name	Description
7:6	RG_VBAT_CC_VTH	**Battery CC dection threshold** 00: 3.3V 01: 3.35V 10: 3.4V 11: 3.45V (default)
4:0	RG_VBAT_CV_VTH	**Battery CV dection threshold trimming option, default 4.2V**

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Bit(s)	Name	Description
		this register is used for FT CV threshold trimming and not for customer's fine tuning (pchr_dig should invert MSB bit. otherwise, BC1.1 2.2V threshold would be wrong) 00000:3.7750V 00001:3.8000V 00010:3.8500V 00011:3.9000V 00100:4.0000V 00101:4.0500V 00110:4.1000V 00111:4.1250V 01000:4.1375V 01001:4.1500V 01010:4.1625V 01011:4.1750V 01100:4.1875V 01101:4.2000V(01101, default) 01110:4.2125V 01111:4.2250V 10000:4.2375V 10001:4.2500V 10010:4.2625V 10011:4.2750V 10100:4.3000V 10101:4.3250V 10110:4.3500V 10111:4.3750V 11000:4.4400V 11001:4.4250V 11111: 2.2V (used in BC1.1 application)

0F94 **CHR_CON4** **Charger Control Register 4** **000F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_CS_VTH			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	RG_CS_VTH	**Current sense voltage detection threshold @ Rcs=65mohm** 1111: 70mA 1110: 200mA 1101: 300mA 1100: 450mA (usbdl) 1011: 550mA 1010: 650mA 1001: 700mA 1000: 800mA 0111: 900mA 0110: 1000mA 0101: 1100mA 0100: 1200mA 0011: 1350mA 0010: 1500mA 0001: 1600mA 0000: 2000mA

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0F98 CHR_CON6 Charger Control Register 6 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_VBAT_OV_DET	RG_VBAT_OV_DEG	RG_VBAT_OV_VTH				RG_VBAT_OV_EN
Type										RO	RW	RW				RW
Reset										0	0	0	0	0		1

Bit(s)	Name	Description
6	RGS_VBAT_OV_DET	**VBAT_OV voltage detection.** 0 VBAT voltage < VBAT_OV_VTH 1 VBAT voltage > VBAT_OV_VTH
5	RG_VBAT_OV_DEG	**VBAT OV voltage detection deglitch enable.** 0 no debounce 1 debounce one cycle (1us)
4:2	RG_VBAT_OV_VTH	**Battery over-voltag detection threshold** 000: 4.200V (default) 001: 4.300V 010: 4.400V 011: 4.450V 1xx: 3.800V
0	RG_VBAT_OV_EN	**Battery over-voltag for driving protection (0: disable, 1: enable)**

0F9A CHR_CON7 Charger Control Register 7 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_BATON_TDET_EN						BATON_TDET_EN	RG_BATON_HT_EN_RSV0	RG_BATON_EN
Type								RW						RW	RW	RW
Reset								0						0	0	1

Bit(s)	Name	Description
8	RG_BATON_TDET_EN	**BATON temperature detection enable via AUXADC (gated by CHR_LDO_DET to default 0 in analog domain)** 0: disable temperature detection related TREF power switch 1: enable temperature detection related TREF power switch (SW should enable AUXADC reference buffer before enable this switch) This RG is also used to enable external SWCHR BATON detection.
2	BATON_TDET_EN	**0: N/A** 1: Enable BATON Temperature detection
1	RG_BATON_HT_EN_RSV0	**Battery-On HW high temperature detection** 0: Disabled 1: Enabled
0	RG_BATON_EN	**BATON battery detection comparator enable (gated by CHR_LDO_DET to default 1 in analog domain)** 0: disable 1: enable (Default)

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0F9E CHR_CON9 Charger Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_FRC_CSVTH_USBDL
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_FRC_CSVTH_USBDL	**Force CS DAC detection threshold to maximum in USB download mode** 0: CS_VTH=450mA in USBDL mode 1: CS_VTH=1600mA in USBDL mode

0FA0 CHR_CON10 Charger Control Register 10 0020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_OTG_BVALID_DET	RG_OTG_BVALID_EN					
Type										RO	RW					
Reset										0	1					

Bit(s)	Name	Description
6	RGS_OTG_BVALID_DET	**Indicates if the session for B-peripheral is valid (0.8V<Vth<4V). Here VBUS is connected to CHRIN.** 0: Vbus < 0.8V 1: Vbus > 4V
5	RG_OTG_BVALID_EN	**OTG BValid detection enable (1: enable, 0: disable)**

0FA6 CHR_CON13 Charger Control Register 13 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_CHRWDT_WR				RG_CHRWDT_EN	RG_CHRWDT_TD			
Type								RW				RW	RW			
Reset								0				1	0	0	0	0

Bit(s)	Name	Description
8	RG_CHRWDT_WR	**To reset charger watch-dog timer and update CHRWDT_TD** 0: reset inactive 1: reset active and CHRWDT_TD updated to PCHR_DIG
4	RG_CHRWDT_EN	**Enable setting for charger watch-dog timer** 0 disable 1 enable if (CHR_EN(@CHR_CON0) == 1) Note1: UVLO don't care this bit and will timeout after 3000s Note2: PCHR_TESTMODE can force to control watch-dog enable by using

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Bit(s)	Name	Description
		this bit
3:0	RG_CHRWDT_TD	**Time constant setting for charger watch-dog timer** 0: 4 sec 1: 8 sec 2: 16 sec 3: 32 sec 4: 128 sec 5: 256 sec 6: 512 sec 7: 1024 sec 8~15: 3000 sec

0FAA CHR_CON15 Charger Control Register 15 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RGS_CHRWDT_OUT	RG_CHRWDT_FLAG_WR	RG_CHRWDT_INT_EN
Type														RO	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	RGS_CHRWDT_OUT	**Time-out flag for charger watch-dog timer** Read: 0: No time-out status 1: Time-out status asserted
1	RG_CHRWDT_FLAG_WR	**Clear time-out flag for charger watch-dog timer** Read: 0: N/A (while RGS_CHRWDT_OUT=0) 1: Clear time-out flag while RGS_CHRWDT_OUT=1
0	RG_CHRWDT_INT_EN	**Interrupt enable setting for charger watch-dog timer.** 0: Disabled 1: Enabled

0FAC CHR_CON16 Charger Control Register 16 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_ADCIN_CHR_EN	RG_ADCIN_VSEN_EN	RG_ADCIN_VBAT_EN	RG_ADCIN_VSEN_EXT_BATON_EN	RG_ADCIN_VSEN_MUX_EN					RG_USBDL_SET	RG_USBDL_RST		
Type				RW	RW	RW	RW	RW					RW	RW		
Reset				0	0	0	0	0					0	0		

Bit(s)	Name	Description
12	RG_ADCIN_CHR_EN	**AUXADC input source enable for CHR** 0: Disabled 1: Enabled
11	RG_ADCIN_VSEN_E	**AUXADC input source enable for VSEN**

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Bit(s)	Name	Description
	N	0: Disabled 1: Enabled
10	RG_ADCIN_VBAT_EN	**AUXADC input source enable for VBAT** 0: Disabled 1: Enabled
9	RG_ADCIN_VSEN_EXT_BATON_EN	**AUXADC input source enable for external source to be switched to AUXADC's Ch3** 0: Disabled 1: Enabled
8	RG_ADCIN_VSEN_MUX_EN	**AUXADC input source enable for VSEN to be switched to VBAT's divider** 0: Disabled 1: Enabled
3	RG_USBDL_SET	**USBDL_MODE software set control** 0: No effect 1: Force enter USBDL MODE
2	RG_USBDL_RST	**USBDL_MODE software reset control** 0: No effect 1: Force leave USBDL MODE (priority is less than USBDL_DET)

0FAE CHR_CON17 Charger Control Register 17 0002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_UVLO_VH_LAT			RG_UVLO_VTHL				
Type									RW			RW				
Reset									0			0	0	0	1	0

Bit(s)	Name	Description
7	RG_UVLO_VH_LAT	**UVLO VH Latch Siganl** 0: disabled 1: enabled
4:0	RG_UVLO_VTHL	**UVLO low threshold selection** 00000: 2.5V, 00001: 2.55V, 00010: 2.6V (default), 00011: 2.65V 00100: 2.7V, 00101: 2.75V, 00110: 2.8V, 00111: 2.85V, 01000: 2.9V

0FB0 CHR_CON18 Charger Control Register 18 0003

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_LBAT_INT_VTH				
Type												RW				
Reset												0	0	0	1	1

Bit(s)	Name	Description
4:0	RG_LBAT_INT_VTH	**LBAT_INT threshold voltage** 00000: 2.5V, 00001: 2.55V, 00010: 2.6V (default), 00011: 2.65V 00100: 2.7V, 00101: 2.75V, 00110: 2.8V, 00111: 2.85V, 01000: 2.9V, 01001: 2.95V, 01010: 3.0V, 01011: 3.05V, 01100: 3.1V, 01101: 3.15V, 01110: 3.2V, 01111: 3.25V, 11000: 3.3V, 11001: 3.35V, 11010: 3.4V

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0FB2 CHR_CON19 Charger Control Register 19 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_BGR_UNCHOP	RG_BGR_UNCHOP_PH		RG_BGR_RSEL		
Type											RW	RW		RW		
Reset											0	0		0	0	0

Bit(s)	Name	Description
5	RG_BGR_UNCHOP	**BGR unchop mode.** 0: chop mode 1: unchop mode
4	RG_BGR_UNCHOP_PH	**BGR unchop mode phase selection.** 0: select phase 0 path in the unchop mode. 1: select phase 1 path in the unchop mode.
2:0	RG_BGR_RSEL	**BGR resistor (R0 = R1) selection, R2=85K, and VBG=(R0/R2)*dVBE+VBE** 0: c0, 780K (default) 1: c1, 820K 2: c2, 860K 3: c3, 900K 4: cm4, 620K 5: cm3, 660K 6: cm2, 700K 7: cm1, 740K

0FB4 CHR_CON20 Charger Control Register 20 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_BC11_CMP_OUT				RG_BC11_VSRC_EN		RG_BC11_RST	RG_BC11_BB_CTRL
Type									RO				RW		RW	RW
Reset									0				0	0	0	0

Bit(s)	Name	Description
7	RGS_BC11_CMP_OUT	**Comparison result of BC11 charger detection** 0: DP or DM < BC11_VREF_VTH 1: DP or DM > BC11_VREF_VTH
3:2	RG_BC11_VSRC_EN	**BC11 voltage source. Set VDP_SRC = 0.6V** 0: disable the voltage 1: enable the voltage source to DM 2: enable the voltage source to DP 3: forbidden
1	RG_BC11_RST	**Reset BC11 detection mechanism in PCHR_DIG** 0: No effect 1: BC11 detection mechanism is disabled in PCHR_DIG
0	RG_BC11_BB_CTRL	**Force BC11 charger detection controlled by baseband** 0: BC11 detection by PCHR_DIG (hardware mode)

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Bit(s)	Name	Description
		1: BC11 detection by baseband (software mode)

0FB6 CHR_CON21 Charger Control Register 21 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_BC11_BIAS_EN	RG_BC11_IPU_EN		RG_BC11_IPD_EN		RG_BC11_CMP_EN		RG_BC11_VREF_VTH	
Type								RW	RW		RW		RW		RW	
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	RG_BC11_BIAS_EN	**Enable BC11 detection bias circuit** 0: Disabled 1: Enabled
7:6	RG_BC11_IPU_EN	**BC11 7~15uA pull up current enable** 0: disable the pull-up current 1: enable the pull-up current to DM 2: enable the pull-up current to DP 3: forbidden
5:4	RG_BC11_IPD_EN	**BC11 50~150uA pull down current** 0: disable the pull-down current 1: enable the pull-down current to DM 2: enable the pull-down current to DP 3: forbidden
3:2	RG_BC11_CMP_EN	**BC11 comparator connection** 0: disable the comparator 1: enable the comparator to DM 2: enable the comparator to DP 3: forbidden
1:0	RG_BC11_VREF_VTH	**VREF threshold voltage for comparator** 0: VREF_VTH=0.325V 1: VREF_VTH=1.2V 2 & 3: VREF_VTH=2.6V (for Apple adaptor)

0FBA CHR_CON23 Charger Control Register 23 0024

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_CSDAC_STP				RG_CSDAC_DLY		
Type										RW				RW		
Reset										0	1	0		1	0	0

Bit(s)	Name	Description
6:4	RG_CSDAC_STP	**Current DAC output step timer.** 1/1/2/3/4/5/6/7 code/ per-step
2:0	RG_CSDAC_DLY	**Current DAC output detection delay control.** 16/32/64/128/256/512/1024/2048us (512us default, reuse in HW CV Mode)

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0FBC CHR_CON24 Charger Control Register 24 0044

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CHRIND_DIMMING	RG_CHRIND_ON	RG_LOW_ICH_DB					
Type									RW	RW	RW					
Reset									0	1	0	0	0	1	0	0

Bit(s)	Name	Description
7	RG_CHRIND_DIMMING	**Enable pre-charge indicator dimming** 0: Disabled 1: Enabled
6	RG_CHRIND_ON	**Pre-charge indicator on (gated by CHR_LDO_DET to default 0 in analog domain)** 0: disable indicator 1: enable indicator
5:0	RG_LOW_ICH_DB	**Plug out HW detection debounce time (base=16ms)** Debounce time : Code * 16ms

0FBE CHR_CON25 Charger Control Register 25 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_ULC_DET_EN	RG_HWCV_EN		RG_TRACKING_EN		RG_CSDAC_MODE	RG_VCDT_MODE	RG_CV_MODE
Type									RW	RW		RW		RW	RW	RW
Reset									0	0		1		0	0	0

Bit(s)	Name	Description
7	RG_ULC_DET_EN	**Enable charger plug out auto detection. This fuction has to be applied with RG_HWCV_EN=1.** 0: Disabled 1: Enabled
6	RG_HWCV_EN	**Enable hardware CV current tracking** 0: Disabled 1: Enabled
4	RG_TRACKING_EN	**0 : Current calibration use CS_VTH[n] and CS_VTH[n-1] as high/low threshold.** 1 : Current calibration use CS_VTH[n] and LTH as high/low threshold.
2	RG_CSDAC_MODE	**0: If not entering CC, charging is AUTO mode** 1: If leaving UVLO, charging is controlled by RG_CSDAC_EN (same as CC mode)
1	RG_VCDT_MODE	**Charger detection mode selection** 0: Charger detection can only be active in off state 1: Charger detection is active in both on and off state
0	RG_CV_MODE	**Battery CV detection mode selection.** 0: CV detection can only be active in off state 1: CV detection is active in both on and off state

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0FC8 CHR_CON30 Charger Control Register 30 0055

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DAC_USBDL_MAX									
Type							RW									
Reset							0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
9:0	RG_DAC_USBDL_MAX	**USBDL maximum current setting** Default: 85 ==> 0001010101

0FCA CHR_CON31 Charger Control Register 31 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PCHR_CM_VDEC_STATUS				RG_CM_VDEC_TRIG
Type												RO				RW
Reset												0				0

Bit(s)	Name	Description
4	PCHR_CM_VDEC_STATUS	**Automatic current procedure status in adaptor output voltage decrement communication mode** 0: Idle 1: Previous trigger is done
0	RG_CM_VDEC_TRIG	**Automatic current procedure trigger in adaptor output voltage decrement communication mode** 0: No effect 1: Trigger automatic current procedure in adaptor output voltage decrement communication mode

0FCC CHR_CON32 Charger Control Register 32 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PCHR_CM_VINC_STATUS				RG_CM_VINC_TRIG
Type												RO				RW
Reset												0				0

Bit(s)	Name	Description
4	PCHR_CM_VINC_STATUS	**Automatic current procedure status in adaptor output voltage decrement communication mode** 0: Idle 1: Previous trigger is done
0	RG_CM_VINC_TRIG	**Automatic current procedure trigger in adaptor output voltage increment communication mode** 0: No effect 1: Trigger automatic current procedure in adaptor output voltage increment communication mode

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0FCE **CHR_CON33** **Charger Control Register 33** **1D1D**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VDEC_HPRD2								RG_CM_VDEC_HPRD1					
Type			RW								RW					
Reset			0	1	1	1	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD2	**2nd high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1) x 10ms
5:0	RG_CM_VDEC_HPRD1	**1nd high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1) x 10ms

0FD0 **CHR_CON34** **Charger Control Register 34** **091D**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VDEC_HPRD4								RG_CM_VDEC_HPRD3					
Type			RW								RW					
Reset			0	0	1	0	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD4	**4rd high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1) x 10ms
5:0	RG_CM_VDEC_HPRD3	**3th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1) x 10ms

0FD2 **CHR_CON35** **Charger Control Register 35** **3109**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VDEC_HPRD6								RG_CM_VDEC_HPRD5					
Type			RW								RW					
Reset			1	1	0	0	0	1			0	0	1	0	0	1

Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD6	**6th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1) x 10ms
5:0	RG_CM_VDEC_HPRD5	**5th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1) x 10ms

0FD4 **CHR_CON36** **Charger Control Register 36** **0909**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name			RG_CM_VINC_HPRD2								RG_CM_VINC_HPRD1					
Type			RW								RW					
Reset			0	0	1	0	0	1			0	0	1	0	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD2	**2st high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1) x 10ms
5:0	RG_CM_VINC_HPRD1	**1nd high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1) x 10ms

0FD6 CHR_CON37 Charger Control Register 37 1D1D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VINC_HPRD4								RG_CM_VINC_HPRD3					
Type			RW								RW					
Reset			0	1	1	1	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD4	**4rd high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1) x 10ms
5:0	RG_CM_VINC_HPRD3	**3th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1) x 10ms

0FD8 CHR_CON38 Charger Control Register 38 311D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VINC_HPRD6								RG_CM_VINC_HPRD5					
Type			RW								RW					
Reset			1	1	0	0	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD6	**6th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1) x 10ms
5:0	RG_CM_VINC_HPRD5	**5th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1) x 10ms

0FDA CHR_CON39 Charger Control Register 39 0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_CM_LPRD					
Type											RW					
Reset											0	0	1	0	0	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
5:0	RG_CM_LPRD	**Low pulse width in communication mode** Low pulse width = (Setting+1) x 10ms

0FDC **CHR_CON40** **Charger Control Register 40** **00AF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CM_CS_VTHH				RG_CM_CS_VTHL			
Type									RW				RW			
Reset									1	0	1	0	1	1	1	1

Bit(s)	Name	Description
7:4	RG_CM_CS_VTHH	**Current sense detection high threshold in communication mode** 0000: 2000mA 0001: 1600mA 0010: 1500mA 0011: 1350mA 0100: 1200mA 0101: 1100mA 0110: 1000mA 0111: 900mA 1000: 800mA 1001: 700mA 1010: 650mA 1011: 550mA 1100: 450mA 1101: 300mA 1110: 200mA 1111: 70mA
3:0	RG_CM_CS_VTHL	**Current sense detection low threshold in communication mode** 0000: 2000mA 0001: 1600mA 0010: 1500mA 0011: 1350mA 0100: 1200mA 0101: 1100mA 0110: 1000mA 0111: 900mA 1000: 800mA 1001: 700mA 1010: 650mA 1011: 550mA 1100: 450mA 1101: 300mA 1110: 200mA 1111: 70mA 0: 2000mA 1: 1600mA 2: 1500mA 3: 1350mA 4: 1200mA 5: 1100mA 6: 1000mA 7: 900mA 8: 800mA 9: 700mA 10: 650mA 11: 550mA 12: 450mA

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Bit(s)	Name	Description
		13: 300mA 14: 200mA 15: 70mA

0FDE CHR_CON41 Charger Control Register 41 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_PCHR_RSV							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RG_PCHR_RSV	**Reserved**

0FE0 CHR_CON42 Charger Control Register 42 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_ENVTEM_EN	RG_ENVTEM_D
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_ENVTEM_EN	**To block CHR_DET signal to start_up** 0: N/A 1: write enable
0	RG_ENVTEM_D	**To block CHR_DET signal to start_up** 1:block 0: non-block

0FE4 CHR_CON43 Charger Control Register 43 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CM_VINC_INT_EN		RG_CM_VDEC_INT_EN									
Type					RW		RW									
Reset					0		0									

Bit(s)	Name	Description
11	RG_CM_VINC_INT_EN	**Pump Express VDEC INT en**
9	RG_CM_VDEC_INT_EN	**Pump Express VDEC INT en**

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0FE6 CHR_CON44 Charger Control Register 44 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RGS_BATON_UNDET	RG_QI_BATON_LT_EN
Type															RO	RW
Reset															0	1

Bit(s)	Name	Description
1	RGS_BATON_UNDET	Battery-On undetected (1: not detected, 0: detected)
0	RG_QI_BATON_LT_EN	

0FE8 CHR_CON48 Charger Control Register 48 0C08

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_VCDT_TRIM			
Type													RW			
Reset													1	0	0	0

Bit(s)	Name	Description
3:0	RG_VCDT_TRIM	VCDT trim for 2% viration spec.

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4 Application Notes

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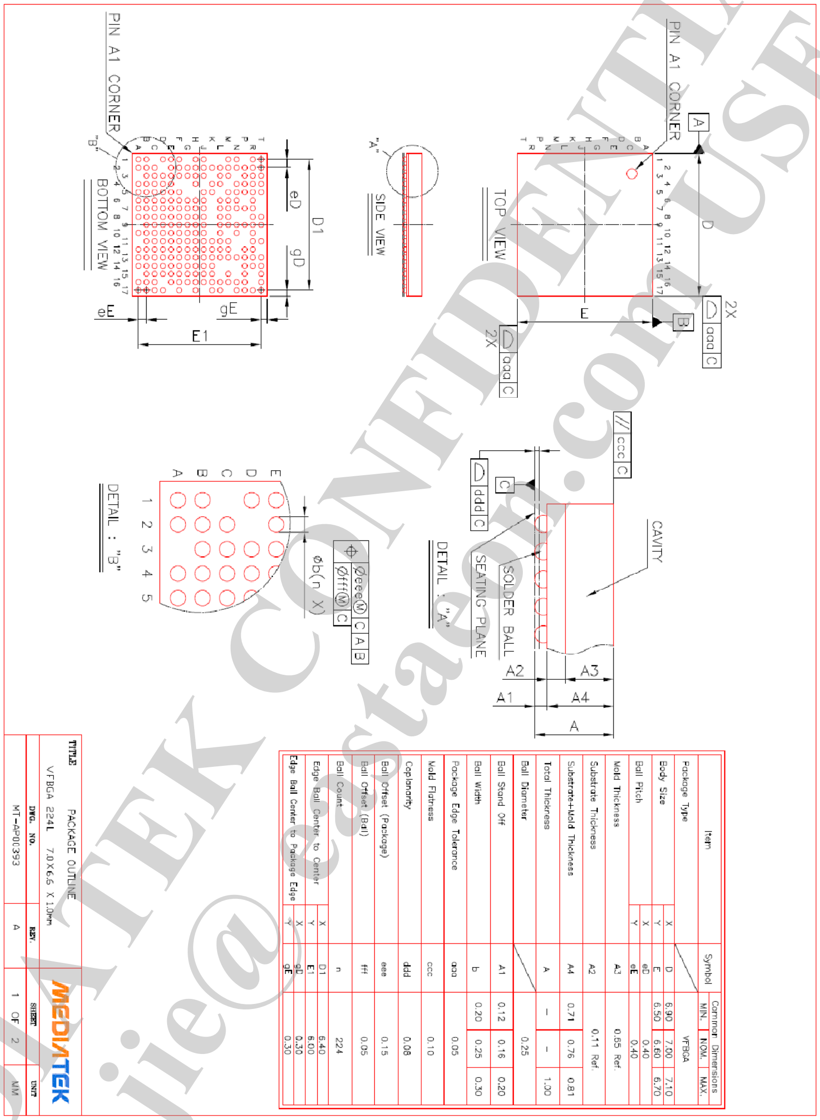
5 MT6353 Packaging

5.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VFBGA	
Body Size	X	D	6.90	7.00	7.10
	Y	E	6.50	6.60	6.70
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		224	
Edge Ball Center to Center	X	D1		6.40	
	Y	E1		6.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

Figure 5-1. Package dimension

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Appendix

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